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A cost-efficient DC active load laboratory solution

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The increased use of DC renewable energy resources and DC storage systems, combined with the necessary reduction of energy waste, is boosting the development of DC smart grids. In this scenario, DC load emulation is of great importance. From the hardware point of view, DC buses stability of smart grids and the different DC/DC converter topologies must be tested. From the software point of view, smart grid strategies and job schedulers must be tested with different power absorption profiles. Moreover, DC load emulation can be useful for many other purposes, such as battery characterization, power supply testing, photovoltaic I-V curve measurements, *etc.* In this work, a cost-efficient DC Active Load (AL) solution is proposed. The principle of the circuit topology is a buck-boost-derived converter. This solution can be designed and tested considering the required voltage, current, and maximum input power. Both simulation and experimental results are shown on a 400 W size prototype. Thermal and electrical results validate the simulation model and the AL feasibility.

KEYWORDS

active load, power supply testing, cost-efficient, load emulation, fast prototyping, arbitrary current absorption, electronic load, thermal management

Introduction

The shift towards the use of renewable energy resources and storage systems boosted the research and development of smart grids with DC buses and small DC/DC voltage converters as point-of-load interfaces. In the literature, different grid architectures can be found with a 48 V DC bus and small DC/DC voltage converters (Kumar et al., 2019; Moussa et al., 2019). Moreover, different control strategies can be applied, i.e. conventional droop control, virtual-resistance-based droop control, and adaptive droop control (Singh et al., 2019). In this scenario, multiple programmable active loads are of great importance for tests with varying power absorption profiles (e.g., for dynamic performance analysis (Zaitsev, 2021; Fu et al., 2022). Constant resistive loads are often unsuitable to ensure a full scenario test of smart grids, particularly for smart control strategies that consider the time-variant power absorption of the connected loads. Moreover, the design of the point-of-load DC/DC converters can sensibly change with the desired output voltage and power ratings. Thereby, this paper proposes a cost-efficient AL solution that can be programmed for a time-varying scenario.

Historically, ALs, known also as electronic loads, are used to test power converters. In comparison to the fixed load impedances, using ALs, a dynamic load change can be emulated to evaluate the converter performances in terms of disturbance rejection. However, in this case, the thermal management of the electronic loads is not an issue due to short-time tests. In the literature, many topologies of AL can be found. Often, they are dissipative and they are made to behave as variable resistors (Rosas-Caro et al., 2009). With a programmable AL the flexibility is higher and many features of a power converter under test, such as load regulation, power supply ratings, and overcurrent protection, can be properly and smoothly tested. Moreover, ALs can be used to test the capacity of batteries (Rathy and Balaji, 2018).

Another very useful application is the testing of power converters to supply digital systems such as microcontrollers or solid-state drives (Williams, 2011; Manjunath I and Dr. V Chayapathy, 2017). Here, a power MOSFET is switched to evaluate the current slew rate with a step load variation.

With the diffusion of smart grids, the use of ALs has been extended. They are used both for AC (single and 3-phase) and DC characterizations of power converters, sources, and buses (Serban et al., 2006; Tsang and Chan, 2012; Peng et al., 2016; Geng et al., 2018; Kanadhiya and Bohra, 2018; Nujithra and Premarathne, 2018; Pudur and Srivastava, 2018; Serna-Montoya et al., 2019; Serna-Motoya et al., 2022). Typically, the ALs topologies for micro and nano grids are based on converters such as boost (Ayop et al., 2021), SEPIC (Vogman and Consulting, 2018), buck-boost (Meng-Ting et al., 2017), back-to-back (Li et al., 2008), and multilevel inverters (Niu et al., 2021).

In this work, an AL topology derived from the buck-boost power converter topology is proposed. The design criterium, unlike the typical one adopted for an interface power converter, is thought for increasing power dissipation. This is reached with a specifically added resistance and inductance on the input section. Working input voltage and power absorption ranges can be easily changed and adapted using the proposed topology.

The prototype has been designed for input voltages in the range 12÷48 V and absorbed currents up to 10 A. Simulations have been validated through experimental results to easily design scaled ALs. Both the static and dynamic behaviors of the AL prototype are shown.

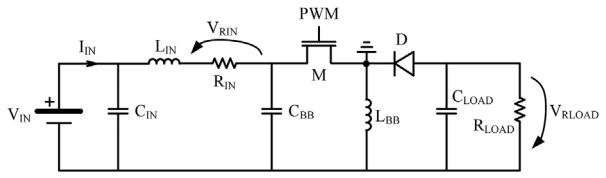

FIGURE 1
Active Load circuit topology.

Active load circuit topology

The topology of the proposed AL is a buck-boost-derived converter, as shown in Figure 1. For AL applications, high efficiency is not a requirement, for this reason, an improved input passive filter and an input resistance for power dissipation sharing are added, and the output capacitors are not sized to reduce the voltage ripple.

The main power dissipation is obtained through the input resistance R_{in} and the load resistance R_{load}. For the first one, the power at the input is strictly related to the input current I_{in} and the resistance value R_{in}, as in Eq. 1. For the load resistance R_{load},

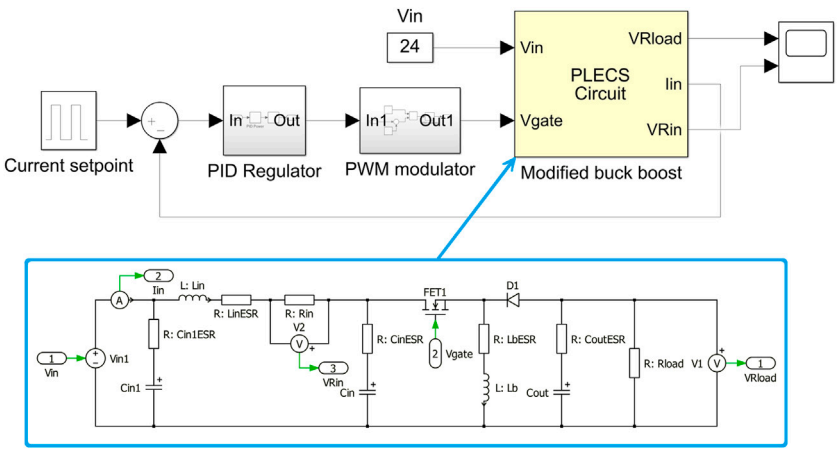

FIGURE 2
Active Load Simulation Model. The PLECS subsystem with the circuit model is highlighted.

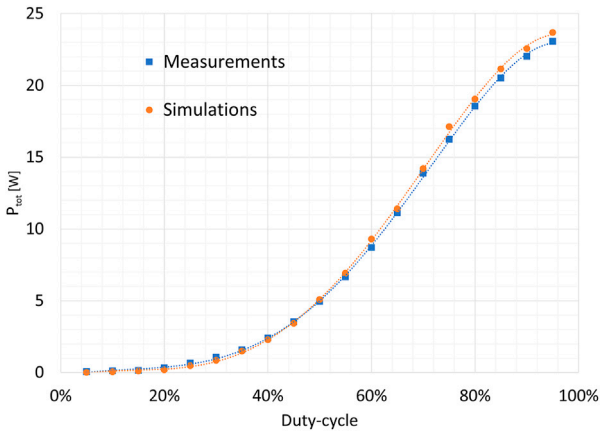

FIGURE 3
Total input absorbed power *versus* the duty-cycle at fixed input voltage V_{in} = 5 V.

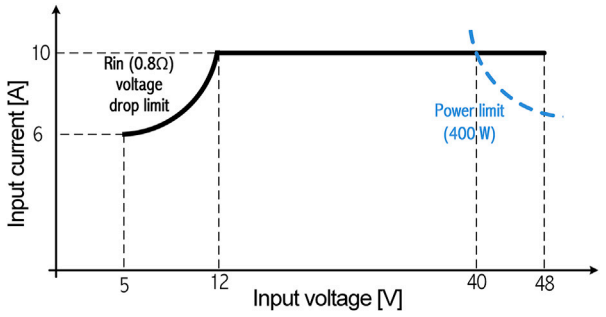

FIGURE 4
Operating V-I limits of the realized prototype.

the power dissipated is related to the duty-cycle (ρ) of the PWM control signal applied to the MOSFET, and both input voltage V_{in} and current I_{in}. If the power dissipated by the switching device and reactive components can be neglected, and continuous conduction mode is assumed, the power dissipated by the load can be represented by Eq. 2.

$$P_{R_{in}} = I_{in}^2 \cdot R_{in} \tag{1}$$

$$P_{R_{Load}} = \frac{\left[\frac{(V_{in} - R_{in} \cdot I_{in}) \cdot \rho}{1-\rho}\right]^2}{R_{Load}} \tag{2}$$

Simulation model and component sizing

For the optimal components sizing, the AL has been simulated in MATLAB/Simulink environment using PLECS blockset for the buck-boost modified scheme. Figure 2 shows the simulation model, where the PLECS subsystem that contains the AL circuit topology is highlighted.

The input resistor R_{in} is sized considering the maximum input current required at the lowest input voltage. Considering a high input current I_{in}, the voltage drop over R_{in} rises, reducing the maximum voltage on the load resistance $V_{R_{\text{load}}}$. On the other side, for high input voltages and input currents, the resistor R_{in} helps to filter the input current and allows higher power dissipation. For an AL prototype useful to emulate variable loads in a nanogrid architecture, we sized the circuit for input voltages between 12 V and 48 V, and input currents up to 10 A. For this reason, we used a 0.8 Ω, 100 W,

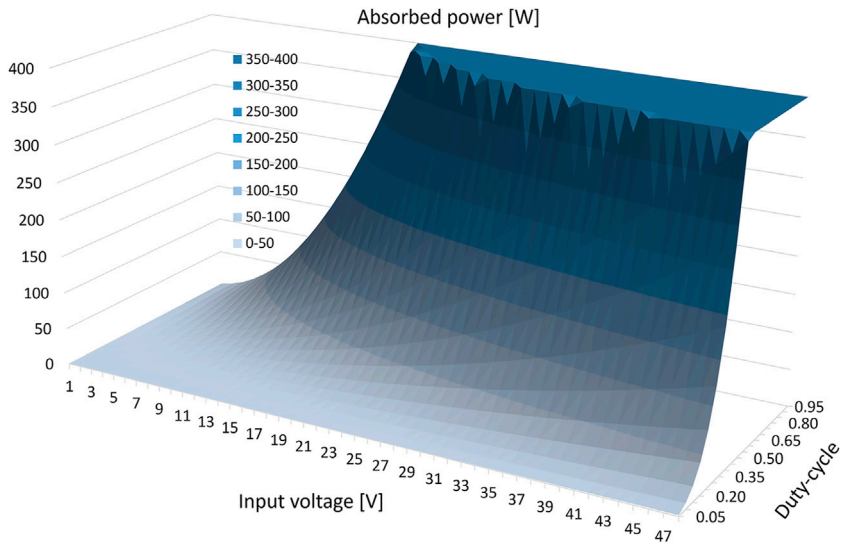

FIGURE 5
Surface plot of the total input absorbed power *versus* the input voltage and the duty-cycle.

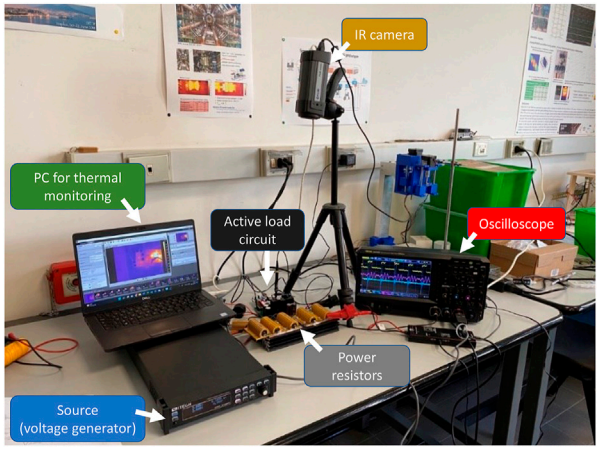

FIGURE 6
Active load circuit test bench.

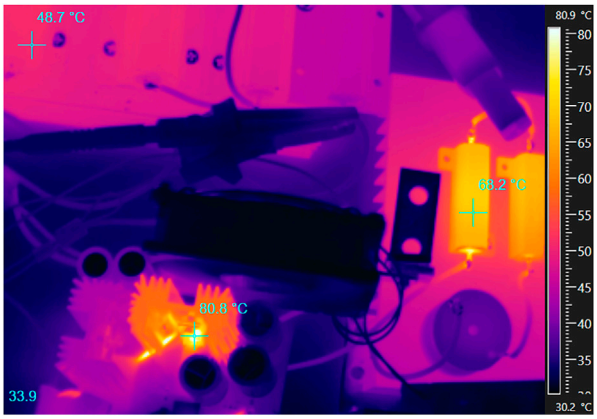

FIGURE 8
Active Load thermal map with input voltage V_{in} = 40 V and input current I_{in} = 10 A (P_d = 400 W).

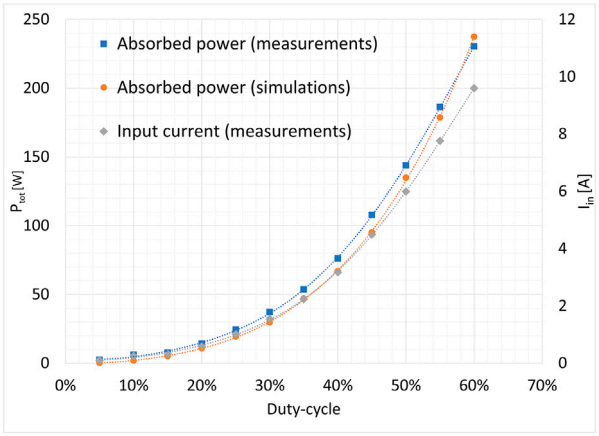

FIGURE 7
Total input absorbed power and input current *versus* the duty-cycle at fixed input voltage V_{in} = 24 V.

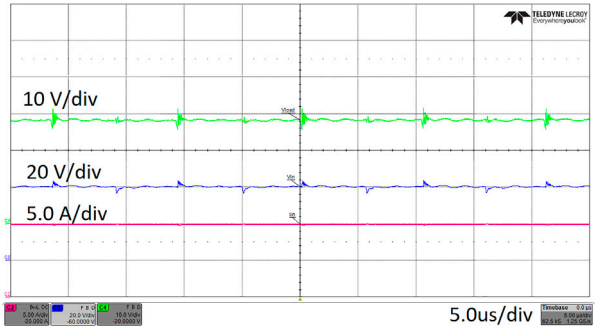

FIGURE 9
Oscilloscope capture with input voltage V_{in} = 40 V and input current I_{in} = 10 A (P_d = 400 W).

input power resistor R_{in}. Considering a 12 V input voltage, the input voltage of the buck-boost circuit can be calculated as $[(V_{in} - R_{in} \cdot I_{in})]$, resulting in a 4 V voltage, which can be boosted on the load resistance to approximately 36 V. Therefore, if an input voltage V_{in} of 5 V is applied, the maximum absorbed power is reduced due to the input resistor R_{in}. Figure 3 shows the dissipated power and current behavior *versus* the duty-cycle at 5 V input voltage.

As for the load resistor R_{load}, the resistance can be determined by Eq. 2, considering the maximum required dissipated power on the load resistance as a function of the input voltage V_{in}, a 0.9 duty-cycle, the maximum required input current I_{in}, and the input resistance R_{in}. The equation for the load resistance calculation is shown in Eq. 3.

$$R_{Load} = \frac{\left[\frac{(V_{in} - R_{in} \cdot I_{in}) \cdot 0.9}{0.1}\right]^2}{P_{R_{Load}}} \quad (3)$$

For our application, with a 12 V input voltage, a 0.8 Ω input resistance, a 10 A required input current, and a power dissipated on the AL of approximately 400 W, the load resistance R_{load} results in a value of about 3.2 Ω. The input V-I characteristic of the realized prototype is shown in Figure 4. The 400 W power limit is derived from a thermal limitation, which can be overcome with the addition of fans or resistors with higher power ratings. Figure 5 shows the surface plot of the absorbed power *versus* both input voltage and duty-cycle, with the power limitation of 400 W.

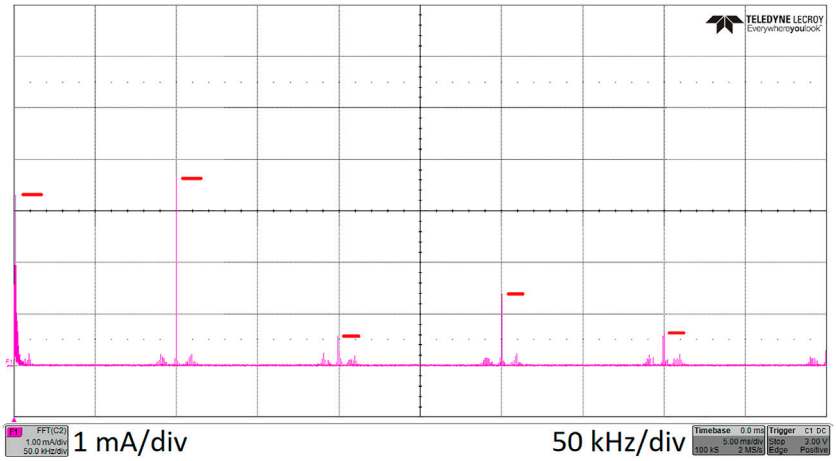

FIGURE 10
FFT of the input current (I_{in} = 10 A) with input voltage V_{in} = 40 V (P_d = 400 W).

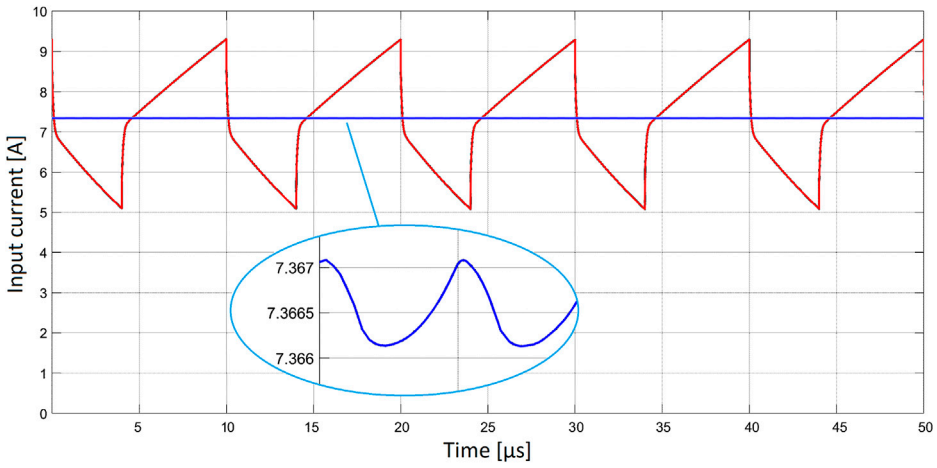

FIGURE 11
Input current comparison between the buck-boost-derived topology (blue) and typical buck-boost converter (red).

Experimental prototype

To validate the simulations, an AL prototype has been developed. The test bench is shown in Figure 6.

The experimental test bench has been defined considering general purpose components already present in a laboratory, and with some layout considerations for a reduced maximum temperature on the circuit and an increased dissipated power. Considering that the power dissipated by the circuit is entirely transformed into heat, the thermal design is a critical issue. The power MOSFET, the diode, and the power resistors need heatsinks for dissipation. In this prototype, also fans have been added, contributing to increase the power dissipation by absorbing power themselves and allowing higher power ratings on the other devices. The fans are turned-on when the input voltage increases over 12 V, and they are fed using an integrated buck converter to reduce the input voltage to a regulated output voltage of 12 V. The two fans blow air on the heatsink of the MOSFET and on the heatsink connected to the input resistance.

The total cost of the proposed AL circuit is around 200 $. This can be considered a very competitive and cost-efficient solution since in the market the costs of programmable electronic loads with similar requirements vary from 750 $ to 1,500 $.

Simulation and experimental results

Simulations have been validated through experimental tests considering two scenarios: an open loop duty-cycle sweep of the PWM control signal with a constant input voltage and a closed loop input current control with a change of the set-point for the dynamic behavior validation.

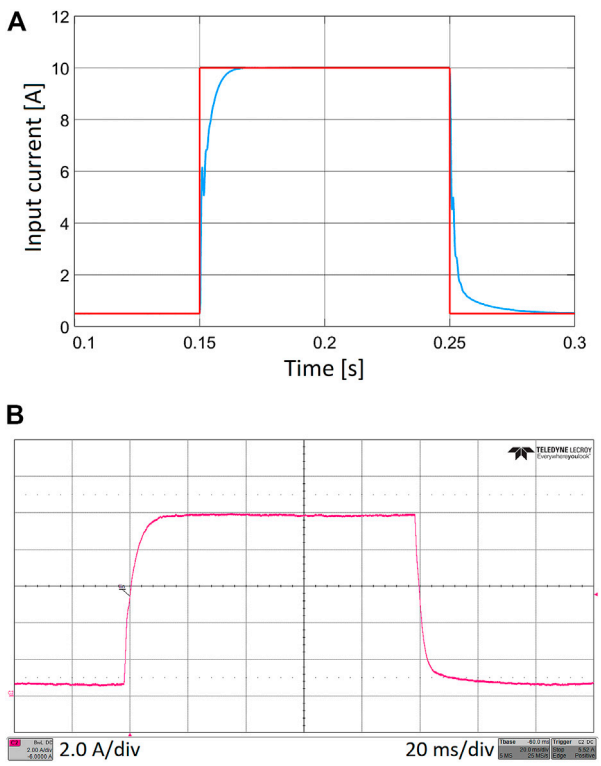

FIGURE 12
Simulation **(A)** end experimental **(B)** results of current step response from I_{in} = 0.5 A–10 A, with fixed input voltage V_{in} = 12 V.

Figure 7 shows the relation between the open loop duty-cycle and both dissipated power and input current with an input voltage of 24 V and as expected this trend is a monotonically increasing function. Waveforms obtained by simulation and measurement are compared.

Figure 8 shows the thermal map with V_{in} = 40 V and dissipated power P_d = 400 W. The hottest temperatures are recorded on the input resistor, the load resistor, and the power MOSFET. High temperatures on the resistors indicate that these components are those where the main heat is generated to dissipate the electrical power absorbed by the AL. While on the MOSFET, the heating is mainly due to a smaller surface for the heat exchange, even though the power dissipated is almost two orders of magnitude smaller than the one on the resistors.

Figure 9 shows the input voltage (blue), the input current (magenta), the voltage drop on the input resistance $V_{R_{in}}$ (green), and the filtered voltage drop on the load resistance $V_{R_{load}}$ (blue). For the input current $I_{in}(t)$ signal quality evaluation, also the FFT of this signal is provided in Figure 10, with an input voltage V_{in} of 40 V and an input current I_{in} regulated at 10 A (total dissipated power of 400 W). The spectrum shows the first harmonic at 100 kHz, exactly the value of the carrier of the PWM signal. The amplitude of the first harmonic is less than 4 mA. All other higher harmonics present a reduced amplitude compared to the first one. These measurements confirm the good behavior of the proposed architecture in terms of input current distortion.

The input current of the proposed buck-boost derived topology can be compared with a classic buck-boost converter. In Figure 11, the simulation results of the input current with two architectures are shown, namely the proposed topology and a buck-boost topology without input

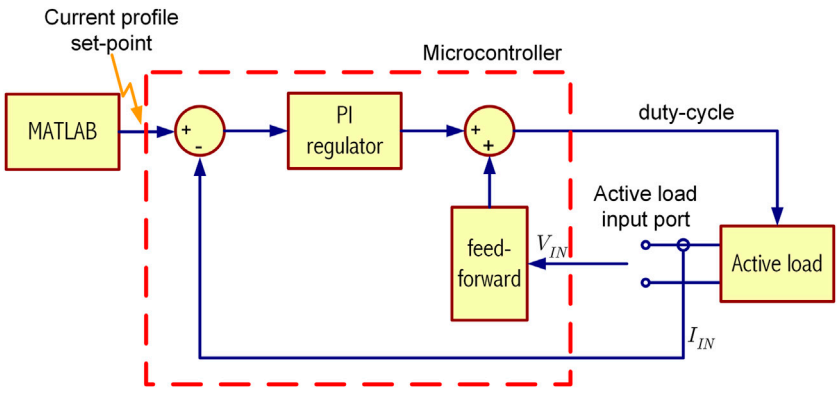

FIGURE 13
Block diagram of the Active Load control algorithm.

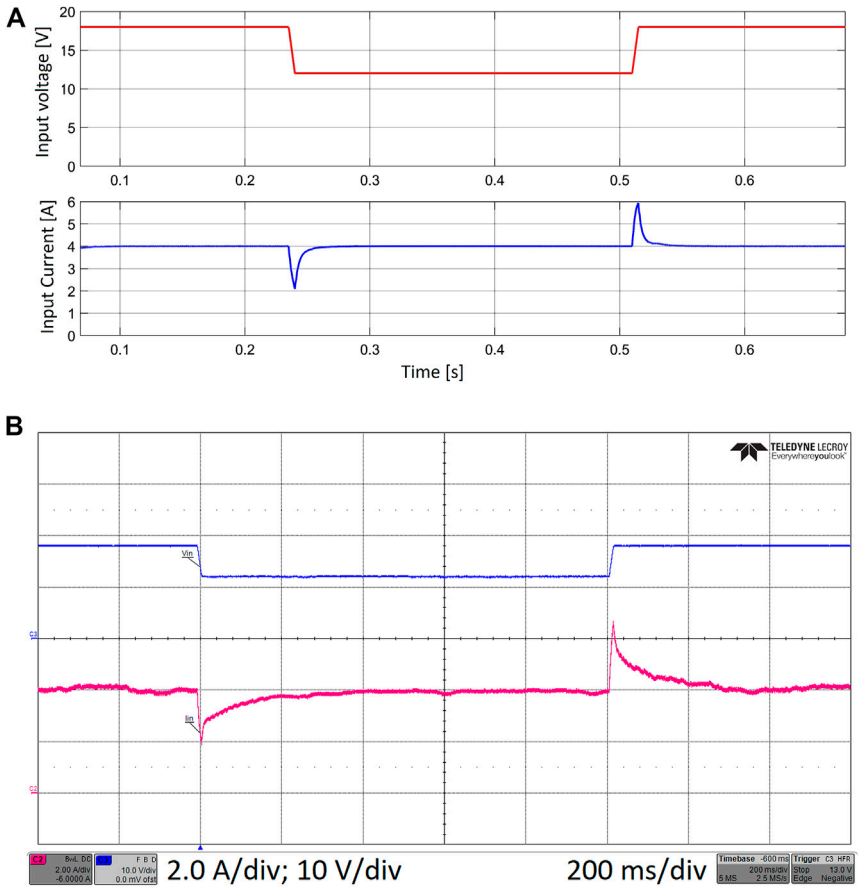

FIGURE 14
Simulation **(A)** and experimental **(B)** results with an input voltage change from V_{in} = 18 V–12 V, with constant input current set-point I_{in} = 4 A.

resistor and inductor, keeping all the other components with the same values. The high current ripple of the classic buck-boost is not suitable for an AL application.

Finally, experimental tests on the prototype have been done to verify the dynamic behavior of the circuit, and results were compared with those obtained using the simulation model. Considering the same PI tuning values for the current control loop, and a 12 V input voltage, Figure 12 shows the simulation results (a) and experimental results (b) with a set-point changing from 0.5 A to 10 A, and from 10 A to 0.5 A. In this configuration, for a current step-up change, a settling time of about 12 m is measured. A higher circuit response time, mainly due to the time necessary to discharge the energy stored in the inductors and capacitors, can be observed for a current step-down change. In this case, a settling time of about 14 m is measured. In both cases, measurements can be compared with simulations, validating the model that can be used also to define the proportional-integral regulator fine tuning.

The proposed solution can receive complex current set-point profiles from a PC *via* MATLAB environment. This operating principle can be used for large-scale emulations, where the microcontroller receives a parameterized set-point sequence at its input. The block diagram of the control algorithm is shown in Figure 13.

Finally, the circuit has been simulated and tested with an input voltage change from 18 V to 12 V, with a 4 A input current constant set-point. Simulation results (a) and experimental ones (b) are shown in Figure 14. These waveforms show a good input voltage change rejection.

Conclusion

This work proposes a cost-efficient programmable DC AL. The DC AL can be used for DC load emulation, DC/DC converter tests, battery characterization, and in general for all the applications where an arbitrary and programmable current

profile absorption is needed. For this realization, a buck-boost-derived topology has been adopted with general-purpose discrete components. The circuit is supervised by a microcontroller which can be interfaced with a PC *via* software for complex current profile load emulations.

Simulations have been used for sizing the components and have been validated through experimental measurements. The prototype has been characterized thermally and electrically. Static current absorption profiles and dynamic input current control behaviors have been first simulated, and then tested. The fabricated prototype works with input voltages from 12 V to 48 V, with input currents up to 10 A, and with a maximum power absorption of 400 W. The total cost of the prototype is around 200 $, which is very competitive with respect to the market available solutions.

Data availability statement

The raw data supporting the conclusion of this article will be made available by the authors, without undue reservation.

Author contributions

All authors listed have made a substantial, direct, and intellectual contribution to the work and approved it for publication.

Conflict of interest

The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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