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Editorial

Low-Voltage Integrated Circuits Design and Application

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One of the most challenging tasks for analog and digital designers is to maintain the circuit performances by developing novel circuit structures, robust, reliable, and capable of operating with low supply voltage.

In recent years, the design of low voltage and ultra-low power circuits is, indeed, of paramount importance. This is motivated by the power constraints and the advanced deep submicron technologies that require lower and lower supply voltages, less than 1 V. Even lower supply voltage may be requested for low-power systems, especially the ones applied in biomedical implantable or wearable electronic devices, autonomous sensor nodes supplied with non-conventional energy sources, the Internet of Things networks, and other similar applications.

This Special Issue consists of twenty-one papers covering a broad range of topics related to the design and applications of low voltage integrated circuits, from analog amplifiers, memories, analog to digital converters, oscillators, transceivers, charge pumps, circuits for signal processing, and beyond.

As the first cluster of applications related to the low voltage "challenge," we can find several circuits dedicated to drive memories and communication circuits. For example, in [1,2], novel back-bias voltage (VBB) generators are proposed to overcome the increasing difficulties in sensing cell data in low-power DRAM. In [3], a novel low-power synchronous preamble data line protocol chip design for serial communication is proposed. The proposed protocol aims to use fewer wires for the interface, reducing the complexity and the area of the chip design. In [4], a method is proposed to increase the read margin in 8T SRAM at lower voltage operation. Traditional 6T SRAM exhibits poor stability with voltage scaling: therefore, in [5], a novel 8T static RAM for reliable subthreshold operation is proposed employing a fully differential scheme.

Low voltage supply has a particularly detrimental effect on the performances of analog circuits. Several works have been devoted to novel circuital schemes to overcome this problem. Analog amplifiers are probably the most important building block in signal processing, and therefore, special attention is devoted to understanding the most critical issues and to propose novel schemes. For example, in [6], a three-stage CMOS amplifier is depicted, which can drive a very large capacitive load. In [7], the susceptibility to Electromagnetic Interference is deeply investigated, and different topologies suited for low voltage supply are compared.

One of the most interesting application fields of ultra-low-power amplifiers is biomedical signal conditioning. In [8], a novel general-purpose biomedical amplifier is proposed, based on flipped voltage follower.

Among the proposed circuital scheme to overcome the detrimental effect of low voltage in analog amplifiers, the most radical approach is probably to implement analog functions through digital blocks, as suggested in References [9,10]. Additionally, in [11], a fast transient digital LDO is proposed and in Reference [12] a time-to-digital converter based on an all-digital voltage controlled oscillator is depicted.

DC/DC converters and power management are an important task in low voltage systems. In [13], regulated charge pumps are compared using Verilog-AMS. In [14], a methodology to early estimate the power consumption of digital circuits is proposed. Analog to digital converters are another important building block. In [15], a power-efficient

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pipelined ADC is proposed. Digital blocks for communications, interfaces, and interconnections are investigated in Reference [16–18]. In [16], a high-speed full-duplex transceiver in 28 nm CMOS technology is proposed. In [17], a low power aviation microsystem is discussed: the proposed chip has the advantage of small size and ultra-low power consumption compared to the traditional PCB circuit design. The work presented in Reference [18] faces the difficulties and challenges of scalable I/Os. In [19], an analog lock-in amplifier with extremely low power consumption is proposed; it is fabricated in a standard 180 nm CMOS process. A convolutional neural network is, instead, the topic of Reference [20].

Finally, in [21], fast and accurate work on new materials is presented: in particular, the results show that by replacing the SiO_2 dielectric mediums with the nanoglass, the maximum reduction of delay time and peak noise voltage is 25.202 ns and 0.102 V for an interconnect length of 3000 µm. The results presented in this paper would be useful to aid in the enhancement of performance of on-chip interconnects and provide guidelines for signal characteristic analysis of interconnection.

From the published papers, which cover an extremely wide area of low voltage, low power integrated circuits, and pleasant reading experience, many ideas could be inspired. This is both in designing novel schematics that can overcome low voltage design problems and in thinking of new technology solutions and new materials, which can face future ICs.

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References

1. Yim, T.; Lee, C.; Yoon, H. High Speed Back-Bias Voltage (VBB) Generator with Improved Pumping Current. *Electronics* **2020**, *9*, 1835. [CrossRef]
2. Lee, C.; Yim, T.; Yoon, H. A Negative Charge Pump Using Enhanced Pumping Clock for Low-Voltage DRAM. *Electronics* **2020**, *9*, 1769. [CrossRef]
3. Chen, S.-L.; Chi, T.-K.; Tuan, M.-C.; Chen, C.-A.; Wang, L.-H.; Chiang, W.-Y.; Lin, M.-Y.; Abu, P.A.R. A Novel Low-Power Synchronous Preamble Data Line Chip Design for Oscillator Control Interface. *Electronics* **2020**, *9*, 1509. [CrossRef]
4. Chang, I.J.; Kang, Y.; Kim, Y. Channel Length Biasing for Improving Read Margin of the 8T SRAM at Near Threshold Operation. *Electronics* **2019**, *8*, 611. [CrossRef]
5. Kim, T.; Manisankar, S.; Chung, Y. A Novel 8T Cell-Based Subthreshold Static RAM for Ultra-Low Power Platform Applications. *Electronics* **2020**, *9*, 928. [CrossRef]
6. Cheng, Q.; Li, W.; Tang, X.; Guo, J. Design and Analysis of Three-Stage Amplifier for Driving pF-to-nF Capacitive Load Based on Local Q-Factor Control and Cascode Miller Compensation Techniques. *Electronics* **2019**, *8*, 572. [CrossRef]
7. Becchetti, S.; Richelli, A.; Colalongo, L.; Kovacs-Vajna, Z. A Comprehensive Comparison of EMI Immunity in CMOS Amplifier Topologies. *Electronics* **2019**, *8*, 1181. [CrossRef]
8. Stornelli, V.; Barile, G.; Leoni, A. A Novel General Purpose Combined DFVF/VCII Based Biomedical Amplifier. *Electronics* **2020**, *9*, 331. [CrossRef]
9. Toledo, P.; Crovetti, P.; Klimach, H.; Bampi, S. Dynamic and Static Calibration of Ultra-Low-Voltage, Digital-Based Operational Transconductance Amplifiers. *Electronics* **2020**, *9*, 983. [CrossRef]
10. Manfredini, G.; Catania, A.; Benvenuti, L.; Cicalini, M.; Piotto, M.; Bruschi, P. Ultra-Low-Voltage Inverter-Based Amplifier with Novel Common-Mode Stabilization Loop. *Electronics* **2020**, *9*, 1019. [CrossRef]
11. Zhang, H.; Wan, P.; Geng, J.; Liu, Z.; Chen, Z. A Fast Transient Response Digital LDO with a TDC-Based Signal Converter. *Electronics* **2020**, *9*, 132. [CrossRef]
12. Mouri Zadeh Khaki, A.; Farshidi, E.; Hamid MD Ali, S.; Othman, M. An FPGA-Based 16-Bit Continuous-Time 1-1 MASH $\Delta\Sigma$ TDC Employing Multirating Technique. *Electronics* **2019**, *8*, 1285. [CrossRef]
13. Ballo, A.; Bottaro, M.; Grasso, A.D.; Palumbo, G. Regulated Charge Pumps: A Comparative Study by Means of Verilog-AMS. *Electronics* **2020**, *9*, 998. [CrossRef]
14. Erdelyi, J.; Macko, D.; Jelemenska, K. PESL: System-Level Estimation of Power-Management Effect on Dynamic Energy Consumption. *Electronics* **2020**, *9*, 1313. [CrossRef]

15. Wan, P.; Su, L.; Zhang, H.; Chen, Z. A Power-Efficient Pipelined ADC with an Inherent Linear 1-Bit Flip-Around DAC. *Electronics* **2020**, *9*, 199. [CrossRef]
16. Ebrahimi Jarihani, A.; Sarafi, S.; Koeberle, M.; Sturm, J.; Tonello, A.M. A 16 Gbps, Full-Duplex Transceiver over Lossy On-Chip Interconnects in 28 nm CMOS Technology. *Electronics* **2020**, *9*, 717. [CrossRef]
17. Lv, H.; Zhang, S.; Han, W.; Liu, Y.; Liu, S.; Chu, Y.; Zhang, L. Design and Realization of an Aviation Computer Micro System Based on SiP. *Electronics* **2020**, *9*, 766. [CrossRef]
18. Bae, W. Supply-Scalable High-Speed I/O Interfaces. *Electronics* **2020**, *9*, 1315. [CrossRef]
19. Maya, P.; Calvo, B.; Sanz-Pascual, M.T.; Osorio, J. Low Cost Autonomous Lock-In Amplifier for Resistance/Capacitance Sensor Measurements. *Electronics* **2019**, *8*, 1413. [CrossRef]
20. Peluso, V.; Rizzo, R.G.; Calimera, A. Performance Profiling of Embedded ConvNets under Thermal-Aware DVFS. *Electronics* **2019**, *8*, 1423. [CrossRef]
21. Xu, P.; Pan, Z.; Tang, Z. The Ultra-Low-k Dielectric Materials for Performance Improvement in Coupled Multilayer Graphene Nanoribbon Interconnects. *Electronics* **2019**, *8*, 849. [CrossRef]