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Abstract: The 4-leg inverter can adjust the load current or output voltage even under unbalanced load conditions, but it is known that the additional switch arm to the 3-leg inverter can increase the overall cost and the failure rate. This paper aims to analyze the failure rate and mean time between failures (MTBF) of 3-leg inverters and 4-leg inverters using part count failure analysis (PCA) and fault-tree analysis (FTA), and to compare the price of the inverters. The FTA can analyze the failure rate, including the type, number and connection status of the circuit components, and moreover the redundancy effect of the 4-leg inverter. For more accurate failure-rate prediction, the failure rate and MTBF of the 4-leg inverter according to the lifecycle of the controller are analyzed. Finally, by comparing the price of 3-leg inverters and 4-leg inverters using the cost model of major parts, the degree of reliability improvement against price increase is quantitatively analyzed.

Keywords: cost model; economic efficiency; 4-leg inverter; failure rate; fault-tree analysis (FTA); mean time between failures (MTBF); part count failure analysis (PCA); 3-leg inverter

1. Introduction

An inverter is a power converter that converts DC into AC, which allows simultaneous control of output voltage and frequency, and is used for various purposes such as motor drives based on VVVF (variable voltage and variable frequency) and grid-connection based on CVCF (constant voltage and constant frequency) control. Among the inverter circuit topologies, the three-phase 3-leg inverter is widely used as a power converter that connects distributed generation (DG) such as solar power, wind power or energy storage systems (ESS) to the grid [1-5]. However, if a DG network accident results in a current imbalance in the three-phase distribution network, the 3-leg inverter cannot supply an imbalanced current called a zero-sequence current. In this case, a 3-leg inverter employing a split DC-link capacitor or a 4-leg inverter can be a good alternative [6–10]. The 3-leg inverter with split DC-link capacitors works like that of three independent half-bridge inverters. Therefore, the line-to-neutral output voltage is half the input voltage, so the utilization of the input voltage becomes low, and moreover the DC-link capacitor directly handles the current flowing to the ground, so large capacitance is required [6,7]. The 4-leg inverter increases the switching loss by the added switch arm. Nevertheless, various modulation techniques are being studied because of the advantages of increasing DC-link voltage utilization [8–10] and the presence of 16 switching states, enabling output voltage adjustments for unbalanced loads and control of energy flow for each phase [11-18].

Three-dimensional space vector modulation (3D SVPWM), an extension of twodimensional space vector modulation (2D SVPWM), was proposed, and 3D SVPWM was extensively studied [11–15]. A carrier-based PWM scheme using offset voltage has



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/). been proposed to alleviate the complexity of 3D SVPWM [16,17]. This research focuses only on the CPWM, which corresponds to class I of the 3D SVPWM, which has the effect of improving the THD but reduces the lifecycle of the inverter because each switch arm has a different power loss due to an unbalanced current. The above-mentioned 4-leg inverter modulation schemes commonly use 16 switching states appropriately to achieve various control objectives. In particular, the 4-leg inverter is capable of alternative operation even if a problem occurs with one switch arm of the 3-legs. In general, from a reliability perspective, increasing the number of parts increases the failure rate, but applying a control technique that takes into account the redundancy to a 4-leg inverter structure can lower the failure rate, which can predict the effect of improving reliability.

The reliability and economics of three-phase 3-leg and 4-leg inverters are analyzed in this paper by using the fault-tree analysis (FTA) technique, which can consider operational characteristics according to the redundancy characteristics of the 4-leg inverter. This study aims to accurately predict reliability according to the driving environment by analyzing the failure rate and MTBF (mean time between failures) by designing the fault-tree reflecting the operational risk according to the 3-leg and 4-leg inverter structure and control method. Among the various control methods for controlling the 4-leg inverter, the analysis is made by adding a redundancy function to the SVPWM method that can produce an increased output voltage compared with the sinusoidal PWM control method while keeping the switching frequency constant.

In this paper, we first define the failure of 3-leg and 4-leg inverters, and then design a fault-tree taking into account the operational characteristics. Second, using the fault library of MIL-HDBK-217F, we calculate the failure rate and the MTBF from the fault-trees. Third, we assume the lifecycle of the controller is 3 to 20 years and reflect this in the fault-tree to analyze the correlation between the lifecycle of the controller and the failure rate of the inverter. Fourth, we calculate the failure rate according to the part count failure analysis (PCA) method and compare it with FTA (fault-tree analysis) results to compare the advantages and disadvantages of 3-leg and 4-leg inverters in terms of reliability. Finally, through the economic analysis of 3-leg and 4-leg inverters, the overall cost is compared to the effect of reliability improvement.

2. Three-Phase 3-Leg and 4-Leg Inverter

2.1. 3-Leg Inverter

The three-phase inverter generates a three-phase AC output voltage using a DC input source to supply power to the three-phase load. Figure 1 shows the circuit configuration of a three-phase 3-leg inverter. The 3-leg inverter consists of three switch arms that can operate independently of each other, and each arm produces its own arm voltage v_A , v_B , v_C for three phases, where the reference for each arm voltage is determined as the potential of the N node corresponding to the (–) potential of the input voltage source. In this case, each arm voltage will be a momentary V_{DC} or zero potential. The line-to-line voltage supplied to the load is $v_{AB} = v_A - v_B$, $v_{BC} = v_B - v_C$, $v_{CA} = v_C - v_A$, so the arm voltage is one of the two values of $\{V_{DC}, 0, -V_{DC}\}$.



Figure 1. Circuit configuration of three-phase 3-leg inverter.

If the three-phase load is balanced, the phase voltage of the load has V_{DC} or 0, and each phase of the load is connected to either of these two voltages. Therefore, if one switch arm fails, an imbalance of power supplied to the three-phase load is inevitable.

2.2. 3-Leg Inverter Employing Split DC-Link Capacitor

To compensate for these unbalanced problems, a 3-leg inverter circuitry with split DC-link capacitors can be used as shown in Figure 2. A three-phase 3-leg inverter with split DC-link capacitors consists of three switch arms that can operate independently of each other and each arm produces its own arm voltage v_A , v_B , v_C for three phases. Here the reference potential for each arm voltage is determined by the neutral point of the series-connected capacitor. In this case, each arm voltage will be a momentary $V_{DC}/2$ or $-V_{DC}/2$. The line-to-line voltage supplied to the load is $v_{AB} = v_A - v_B$, $v_{BC} = v_B - v_C$, $v_{CA} = v_C - v_A$, so the arm voltage is one of the two values of $\{V_{DC}/2, -V_{DC}/2\}$ and the three-phase line voltage is one of the three values of $\{V_{DC}, 0, -V_{DC}\}$.

In Figure 2, the neutral point current flows through the DC-link capacitor, and the ground is clamped by half the DC-link voltage. The 3-leg inverter with split DC-link capacitors is the same as the three half-bridge inverters being driven independently. Therefore, the line-to-neutral output voltage is half the input voltage, so the utilization of the input voltage source is low, and moreover the DC-link capacitor directly handles the current flowing to the ground, so the capacitance increases unrealistically. In conclusion, it is possible to supplement the load imbalance problem, but in the case of a switch arm failure, it is impossible to operate an alternative operation to secure redundancy.

2.3. 4-Leg Inverter

Figure 3 shows the circuit configuration of the 4-leg inverter. The additional switch arm controls the neutral voltage and the neutral current. This allows the 4-leg inverter to generate three independent output voltages regardless of load conditions. In other words, even if one switch arm fails, it is possible to secure 100% redundancy that allows alternative switching operation.



Figure 2. Circuit configuration of three-phase 3-leg inverter employing split DC-link capacitors.



Figure 3. Circuit configuration of three-phase 4-leg inverter.

To compare the reliability of 3-leg and 4-leg inverters, this chapter calculates the failure rate and MTBF (mean time between failures) through part count failure analysis (PCA) and fault-tree analysis (FTA) under conditions where the inverters are controlled by the SVPWM. Figure 4 shows the power stage of the 4-leg inverter and the controller based on TMS320F2835. Table 1 represents the specification of the 4-leg inverter and the 3-leg inverter is constructed using the same component. The types and number of parts that make up the inverter and controller vary widely. Reliability and economics are analyzed for relatively expensive parts, such as the main components IGBT (Insulated Gate Bipolar Transistor), capacitors and inductors, because it is difficult to consider all components in reality. For capacitors, we analyze the electrolytic capacitor of DC-link and the film capacitor for filtering purpose. Supercapacitor can also be analyzed as important parts of the inverter depending on its application area [19], but it is excluded because it is difficult to analyze accurately due to a lack of experimental data.



(a)

(b)

Figure 4. Photograph of three-phase 4-leg inverter: (a) Power stage; (b) controller.

Table 1. Sp	pecifications of	three-phase 4-	leg inverter.
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Item	Values
Output power	100 kW
Output voltage (line-to-neutral)	380 V, 60 Hz
DC-link voltage	600 V
DC-link capacitance	15.5 mF
Switching device	IGBT CM600HA-24H
ac filter for A, B, C phase legs	660 µH
ac filter inductor for neutral leg	330 µH
ac filter capacitor for each phase	150 μΗ

3.1. Calculation of Part Failure Rate by MIL-HDBK-217F

To calculate the failure rate of inverters using PCA and FTA, it is first necessary to calculate the failure rate of parts for the IGBT, the capacitor the and inductor, which are the main circuit components that consist of the inverter. In this paper, we use the fault library of MIL-HDBK-217F, which provides a failure-rate calculation equation for each part [20,21]. It considers various factors such as basic failure rate, power capacity, voltage rating, application, temperature, environment, quality factor, etc. The experimental Equations (1)–(6) are the result of reflecting the specification given in Table 1 for MIL-HDBK-217F's failure-rate calculation formula; the quality factor is based on the commercial product and the environment factor is based on the state in which the inverter is a controlled environment.

3.1.1. Failure Rate of IGBT

The MIL-HDBK-217F does not provide failure rates for IGBTs. Since IGBT consists of series combinations of BJT and MOSFET equivalent, failure of either will result in failure of IGBT. Therefore, the failure rate of IGBT is calculated through the OR-gate operation of the two elements [22].

$$\lambda_{\text{IGBT}} = 1 - (1 - \lambda_{\text{BJT}})(1 - \lambda_{\text{MOSFET}}) \text{ failures/10}^{6} \text{h}$$
(1)

$$\lambda_{\rm BJT} = 0.00076923 (P_r)^{0.37} \exp\left(\frac{V_{CE_applied}}{V_{CEO_rated}}\right) \exp\left[-2114\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right] \text{ failures}/10^6 \text{ h}$$
(2)

$$\lambda_{\text{MOSFET}} = 3.96 \exp\left[-1925\left(\frac{1}{T_J + 273} - \frac{1}{298}\right)\right] \text{ failures}/10^6 \text{ h}$$
 (3)

where (2) and (3) are the failure rate based on the experimental data of BJT and MOSFET, respectively. Here, T_J is the junction temperature (°C), P_r is the rated power (W), $V_{CE-applied}$ is the collector–emitter applied voltage, $V_{CEO-rated}$ is the collector–emitter rated voltage in the base open state.

3.1.2. Failure Rate of DC-Link Capacitor

The failure rates of electrolytic capacitors (aluminum oxide) used as DC-link capacitors are given in (4).

$$\lambda_{C_dc} = 0.012(C)^{0.23} \left[\left(\frac{V_{operating}}{0.6V_{rated}} \right)^5 + 1 \right] \exp\left[\frac{-0.35}{8.617 \times 10^{-5}} \left(\frac{1}{T + 273} - \frac{1}{298} \right) \right] \text{ failures} / 10^6 \text{h}$$
(4)

Equation (4) is the failure rate based on the experimental data of an electrolytic capacitor. Here, *C* is the capacitance (μ F) of the capacitor. V_{operating} is the working voltage of the capacitor, the sum of the DC voltage and AC voltage peak applied to the capacitor, and V_{rated} is the rated voltage of the capacitor. *T* is the ambient temperature (°C) of the capacitor.

3.1.3. Failure Rate of Filter Capacitor

The metalized polypropylene film capacitor is employed as an AC filter capacitor, and the failure rate according to the experimental data is shown in (5).

$$\lambda_{C_f} = 0.051(C)^{0.09} \left[\left(\frac{V_{operating}}{0.6V_{rated}} \right)^5 + 1 \right] \exp\left[\frac{-0.15}{8.617 \times 10^{-5}} \left(\frac{1}{T + 273} - \frac{1}{298} \right) \right] \text{ failures} / 10^6 \text{ h}$$
(5)

Equation (5) is the failure rate based on the experimental data of the metalized polypropylene film capacitor. Here, *C* is the capacitance (μ F) of the capacitor. V_{operating} is the working voltage of the capacitor, the sum of the DC voltage and AC voltage peak applied to the capacitor, and V_{rated} is the rated voltage of the capacitor. *T* is the ambient temperature (°C) of the capacitor.

3.1.4. Failure Rate of Filter Inductor

The failure rate of the AC filter inductor according to experimental data is given in (6).

$$\lambda_L = 0.00054 \exp\left[\frac{-0.11}{8.617 \times 10^{-5}} \left(\frac{1}{T_{HS} + 273} - \frac{1}{298}\right)\right] \text{ failures}/10^6 \text{h}$$
 (6)

$$T_{HS} = T_A + 1.1(\Delta T) \tag{7}$$

Here, the hot spot temperature of the inductor T_{HS} (°C) is calculated by (7). T_A is the ambient temperature (°C) at which the inductor operates and ΔT is the average temperature rise above the ambient temperature (°C).

3.2. Failure Rate by Part Count Failure Analysis (PCA)

Figure 5 shows the failure dependence of a 3-leg inverter in application to PCA. Failure of 3-leg inverter is caused by failure of six IGBTs, a DC-link capacitor, three AC filter capacitors, three AC filter inductors and output load failure. If any of the components fails, it has an OR-gate dependency that leads to a failure of the 3-leg inverter. We calculate the failure rate of the 3-leg inverter by substituting the part failure rate calculated as MIL-HDBK-217F for the failure dependence shown in Figure 5. Here, the output load failure rate reflects 1% of AC filter inductor with the lowest failure rate among key components to minimize the impact on the inverter failure rate under analysis and to reflect some portions of the effect of temperature rise [23–25].

Figure 6 shows the failure dependence of a 3-leg inverter with split DC-link capacitors. Failure of the inverter is caused by failure of six IGBTs, two DC-link capacitors, three AC filter capacitors, three AC filter inductors and output load failure. If any of the components fails, it has an OR-gate dependency that leads to a failure of the inverter.



Figure 5. Failure dependency of three-phase 3-leg inverter.



Figure 6. Failure dependency of three-phase 3-leg inverter with split DC-link capacitors.

Figure 7 shows the failure dependence of a 4-leg inverter. Failure of 4-leg inverter is caused by failure of eight IGBTs, a DC-link capacitor, three AC filter capacitors, three AC filter inductors, a neutral inductor and output load failure. If any of the components fails, it has an OR-gate dependency that leads to a failure of the 4-leg inverter. It is a configuration in which two IGBTs and one neutral inductor are added compared to a 3-leg inverter.

Figure 8a shows a comparison of the failure rate of the three-phase inverters by the PCA method. The 4-leg inverter has the highest failure rate at 25~180 °C. At 25 °C, the failure rate of the 3-leg inverter is 0.243 failures/10⁴h, and the Split DC-link capacitor 3-leg inverter shows 0.245 failures/10⁴h, but the 4-leg inverter represents a relatively high failure rate of 0.307 failures/10⁴h. The increased failure rate of approximately 0.065 failures/10⁴h



compared to 3-leg inverters is the result of an increase of two IGBTs. The difference in failure rates is reduced by 32% at 180 $^{\circ}$ C to approximately 0.021 failures/10⁴h.

Figure 7. Failure dependency of 4-leg inverter.





Figure 8. Comparison of failure rate and mean time between failures (MTBF) by part count failure analysis (PCA): (**a**) Failure rate; (**b**) mean time between failures.

Figure 8b shows the MTBF of a 3-leg inverter at 25 °C is 4.7 years, the split DC-link capacitor 3-leg inverter is 4.66 years, but the 4-leg inverter represents a relatively small MTBF of 3.71 years. The difference in MTBF is about 0.99 years at 25 °C and decreases to about 0.025 years at 180 °C. The reason why the difference in failure rates decreases as the temperature increases is that at higher driving temperatures, the effect of increasing failure rates by temperature is greater than that by the number of parts.

3.3. Failure Rate by Fault-Tree Analysis (FTA)

This chapter designs and analyzes fault-trees for reliability analysis considering the operational characteristics of 3-leg inverters and 4-leg inverters. The design of a fault-tree requires an analysis of the various causes and consequences of failure of the inverter [26–28]. The causes of failure and the effects of the failure are very complex, so it is very difficult to consider all conditions. Therefore, we design a fault-tree for major failures with high RPN (Risk Priority Number) values defined by the multiplication of severity, frequency of occurrence and detectability of failures in FMECA (Failure Mode, Effects Analysis and Criticality Analysis) [29,30].

Fault-Tree Analysis (FTA) is a quantitative failure analysis method that logically analyzes the cause of failures and makes a fault-tree and uses it to obtain the probability of failure. The FTA is a top-down approach that uses Boolean algebra (AND, OR-gate, etc.) in graphical representations to express logical inter-relationships between basic and top events.

3.3.1. Fault-Tree Design of 3-Leg Inverter

Figure 9 shows the fault-tree of a three-phase 3-leg inverter. Failure of the 3-leg inverter is defined as failure of the output voltage generation function. Since the top-level failure of the 3-leg inverter is defined as a failure of the output voltage generation, the cause of the lower stage failure may be the failure of each phase voltage control. Function failures that control the amplitude and frequency of the output voltage are defined as failures on each phase, not separately classified. In addition, the input of the 3-leg inverter is assumed to be supplied by the DC-link capacitor, and the probability of failure of the front-end system supplying power to the DC-link capacitor is included in the DC-link capacitor failure. The main goal is to analyze the reliability of the 3-leg inverter itself. Therefore, the type and condition of the load are treated as a failure of Output load failure] without being specifically identified.

[DC-link power supply failure] consists of OR-gate combination of [DC-link capacitor intrinsic function failure] and [DC-link front-end circuit function failure]. The electrolytic capacitor, which is a DC-link capacitor, is responsible for charging and discharging functions for maintaining DC-link voltage, but may lose its original function due to short circuit, opening and failure of the capacitor itself. Therefore, sub-failures are designed with [Capacitor short failure], [Capacitor open failure] and [DC-link failure]. Since the input of the 3-leg inverter assumes that it is supplied by the DC-link capacitor, the probability of failure of the front-end system supplying power to the DC-link capacitor is included in the DC-link capacitor failure.

[IGBT switching function failure] occurs from the loss of switching function of the upper and lower IGBT of each arm. The causes of $[Q_{xp}$ switching function failure] can be seen as [IGBT intrinsic function failure] and [Switching signal generation failure]. [IGBT intrinsic function failure] is caused by short circuit, open circuit, overheating due to loss of heat-sink function and failure of IGBT itself. Therefore, the sub-event of $[Q_{xp}$ switching failure] is designed as an OR-gate combination of [IGBT Q_{xp} failure], [Short circuit failure], [Open circuit failure] and [Heat-sink failure].

The causes of failure for generating a switching signal of [switching signal generation function failure] are control IC failure, failure of control algorithm and failure of gate-amp. Therefore, the sub-event of [Switching signal generation failure] is designed with OR-gate combination of [Gate-amp function failure], [Control signal generation failure] and [Control IC failure]. [Control signal generation failure] is due to a problem with the control

algorithm itself or to failure of the feedback function due to failure of the PT, CT sensor, etc. Therefore, the sub-event of [Control signal generation failure] is designed as an OR-gate combination of [Control Algorithm failure] and [Feedback function failure].

[AC filtering function failure] consists of the OR-gate combination of [AC filter L_{fx} failure] and [ac filter C_{fx} failure]. The inductor and capacitor located at the output stage of each phase are responsible for generating high quality output voltage by LC filtering the inverter output voltage. While there are many possible causes of failure, only the inductor and capacitor itself are considered as they have relatively low failures compared to IGBT, DC-link capacitors and others.



Figure 9. Fault-tree of three-phase 3-leg inverter.

3.3.2. Fault-Tree Design of 3-Leg Inverter Employing Split DC-Link Capacitors

Figure 10 shows a fault-tree of three-phase 3-leg inverter employing split DC-link capacitors. Another DC-link capacitor is added compared to the 3-leg inverter in Figure 9, adding a red dotted box, an event indicating a failure of that function. This shows that each capacitor failure is designed to be reflected, taking into account the structure of the split DC-link capacitor. An increase in failure rate can be expected as much as an electrolytic capacitor, a DC-link capacitor, compared with the failure rate of a 3-leg inverter.



Figure 10. Fault-tree of three-phase 3-leg inverter with split DC-link capacitors.

3.3.3. Fault-Tree Design of 4-Leg Inverter

Figure 11 shows the fault-tree of a 4-leg inverter. Failure of the 4-leg inverter is defined as failure of the output voltage generation function like that of 3-leg inverter. The red dotted box represents an [IGBT switching function failure] event, which differs from the 3-leg inverter in the fault-tree of a 4-leg inverter. The 4-leg inverter is a structure in which one switch arm is added to the 3-leg inverter. Thus, even if a failure of the IGBT responsible for each phase occurs, the output compensation of the load phase voltage can be achieved through the alternate switching control of the added switch. If the 4-leg inverter meets the 100% redundancy condition, the added switch arm operates completely separate for positive (+) and negative (-) output phase voltage, so the sub-event of [IGBT switching function failure] is designed with OR-gate combination. [Positive (or negative) output voltage generation failure] is designed as AND-gate combination of [Q_{ap} (or Q_{an}) switching function failure] and [Q_{fp} (or Q_{fn}) switching function failure] taking into account 100% redundancy condition.



Figure 11. Fault-tree of three-phase 4-leg inverter.

Figure 12 shows the phase current (i_a, i_b, i_c) and neutral point current (i_n) of the 4-leg inverter. Figure 12a shows each phase current waveform in a balanced three-phase load. It has the same amplitude of the phase current and a neutral current is zero. Figure 12b shows the phase current when the load of phase A is half of the phase B and C loads by load imbalance. The load is balanced by allowing the phase current as much as the reduction of phase A current (i_a) to flow over the additional switch arm. Figure 12c shows the load phase current and neutral current (i_n) when the load of phase C doubles the load of phases A and B due to load imbalance. When the amplitude of the phase C current (i_c) is greater than the current amplitude for the other two phases (i_a, i_b) , the neutral current (i_n) appears to be the same amplitude as the A and B phases but with phase differences. Figure 12d shows a condition in which the phase C current (i_c) cannot flow due to a fault in phase C. The 4-leg inverter, which has the redundancy characteristic, is kept in a balanced three-phase through alternative operation of the additional switch arm.



Figure 12. Phase current (i_a , i_b , i_c) and neutral current (i_n) of three-phase 4-leg inverter: (**a**) With three-phase balanced load condition; (**b**) when the load of phase A is half of the phase B and C loads by load imbalance; (**c**) when the load of phase C doubles phases A and B due to load imbalance; (**d**) alternate operation of the additional switch arm due to failure of phase C.

Figure 13a shows a comparison of the failure rate of the three-phase inverters by FTA. The 4-leg inverter has the lowest failure rate, in the range of 25 to 180 °C. At 25 °C, the 3-leg inverter exhibits 0.247 failures/ 10^4 h, and the split DC-link capacitor 3-leg inverter exhibits 0.254 failures/ 10^4 h, similar to the failure rate results for PCA. However, for 4-leg inverters, the PCA has a failure rate of 0.307 failures/ 10^4 h, but the FTA has a very low failure rate of 0.0266 failures/ 10^4 h. This is because the PCA only considers the type, number and connection of components, but the FTA also considers the operating characteristics of inverters. The 4-leg inverter is a structure in which two IGBT switches with relatively high failure rates are added, but in substance it shows that the added switch arm allows redundancy for each output phase voltage generation, which can significantly reduce the failure rate.

The MTBF in Figure 13b shows that the 3-leg inverter at 25 °C is 4.6 years and the split DC-link capacitor 3-leg inverter is 4.5 years, similar to the results for PCA, but the 4-leg inverter shows a significant increase in lifecycle to about 43 years. However, as the temperature increases, the difference in failure rates decreases compared to PCA results because at higher driving temperatures the effect of increasing failure rates due to temperature is greater than that due to the operating characteristics of the inverter.





Figure 13. Comparison of failure rate and MTBF by fault-tree analysis (FTA): (**a**) Failure rate; (**b**) mean time between failures, year.

3.4. Failure Rate of the Three-Phase Inverter According to the Reliability of the Controller

This section analyzes the failure rate of the inverter according to the reliability of the controller applied to the three-phase inverter. The three-phase inverter can apply various control techniques, such as sinusoidal PWM, SVPWM, depending on the purpose of control. These control algorithms are implemented by control ICs, peripheral circuits, etc., and the severity of failure rates due to performance differences in the control algorithm itself is difficult to assess realistically. Even if performance or complexity between control techniques is considered, the degree of difference in failure rates is not significant and the impact on failure rate analysis is small. Thus, in this paper, the failure of a [Switching signal generation function failure] event corresponding to the controller function in the fault-tree is set to 3, 5, 10, 15 and 20 years and the inverter failure rate and MTBF are analyzed for the analysis of how much the controller including the control algorithm affects the overall reliability of the inverter. Table 2 shows the MTBF converted to failure rate (failures/10⁴h).

Figure 14a shows the failure rate of the 3-leg inverter according to the lifecycle of the controller using the FTA. At 25 °C, it is analyzed as 0.47 failures/ 10^4 h for 20 years, 0.53 failures/ 10^4 h for 15 years, 0.64 failures/ 10^4 h for 10 years, 0.84 failures/ 10^4 h for five years and 0.96 failures/ 10^4 h for three years of controller lifecycle. It shows that the MTBF

of a controller decreases every five years; the failure rate increases almost twice as much. It should be noted that if the MTBF of the controller at 25 °C is less than five years the failure rate of the 3-leg inverter will increase rapidly to 0.84 failures/ 10^4 h. In particular, if the MTBF of the controller is designed to be less than three years, the failure rate of a 3-leg inverter is higher than 0.96 failures/ 10^4 h, indicating that the lifecycle of the controller is a condition that significantly affects the failure rate of the 3-leg inverter.

Table 2. Failure rate of [Switching signal generation function failure] corresponding to MTBF.

MTBF (Year)	MTBF (Day)	MTBF (h)	Failure Rate (Failures/10 ⁴ h)
3	1095	26,280	0.380517504
5	1825	43,800	0.228310502
10	3650	87,600	0.114155251
15	5475	131,400	0.076103501
20	7300	175,200	0.057077626



(a)



Figure 14. Failure rate and MTBF of 3-leg inverter according to the controller lifecycle: (**a**) Failure rate; (**b**) mean time between failures, year.

Figure 14b shows the MTBF of the 3-leg inverter according to the lifecycle of the controller. In order for a 3-leg inverter to obtain MTBF of more than two years at 25 $^{\circ}$ C,

the MTBF of the controller must be guaranteed at least 15 years. In particular, it should be noted that the MTBF of a 3-leg inverter decreases sharply to 1.36 years, if the controller MTBF is less than five years at 25 °C. In operating conditions above 100 °C, it falls below 1.5 years regardless of the MTBF of the controller, as the failure rate increases due to the greater influence on the operating temperature than the lifecycle of the controller.

Figure 15a shows the failure rate of the split DC-link capacitor 3-leg inverter according to the lifecycle of the controller using the FTA. Similar to a 3-leg inverter, the five-year reduction in the controller's MTBF shows that the failure rate almost doubles. If the MTBF of the controller is not more than five years under 25 °C operating conditions, it shall be noted that the failure rate of the split DC-link capacitor 3-leg inverter has increased rapidly to 0.84 failures/10⁴h. In particular, if the MTBF of the controller is designed to be less than three years, the failure rate of the controller is higher than 0.96 failures/10⁴h, similar to the failure rate of the 3-leg inverter, because it significantly affects the failure rate of the inverter.



(a)



Figure 15. Failure rate and MTBF of split-DC-link capacitor 3-leg inverter according to the controller lifecycle: (**a**) Failure rate; (**b**) mean time between failures, year.

Figure 15b shows the MTBF of the split DC-link capacitor 3-leg inverter according to the lifecycle of the controller using the FTA. If the MTBF of the controller is 20 years at 25 °C, the MTBF of the inverter is analyzed to be 2.4 years, 2.13 years for 15 years, 1.79 years for 10 years, 1.36 years for 5 years and 1.19 years for 3 years. The MTBF of the

controller must be guaranteed for at least 15 years in order for the split DC-link capacitor 3-leg inverter to secure MTBF of at least 2 years in operation conditions of 25 °C. At 80 °C and above, the MTBF of the inverter drops to less than 1.5 years regardless of the MTBF of the controller. This is because the failure rate increases due to the greater influence on operating temperature in comparison to the lifecycle of the controller.

Figure 16a shows the failure rate of the 4-leg inverter according to the lifecycle of the controller obtained using the FTA. At 25 °C, it shows a failure rate of 0.07 failures/ 10^4 h when the MTBF of the controller is 20 years, 0.09 failures/ 10^4 h for 15 years, 0.15 failures/ 10^4 h for 10 years, 0.36 failures/ 10^4 h for 5 years, 0.67 failures/ 10^4 h for 3 years. If the lifecycle of the controller is more than 10 years, it is possible to obtain a failure rate of 4-leg inverters according to the MTBF of the controller is analyzed relatively lower than that of 3-leg inverters. This is because the redundancy effect of the 4-leg inverter is greater than that of the lifecycle of the controller.



(a)



Figure 16. Failure rate and MTBF 4-leg inverter according to the controller lifecycle: (**a**) Failure rate; (**b**) mean time between failures, year.

4. Economic Efficiency Analysis of Inverter

In this section, we derive the cost model for the design of the 3-leg inverter and 4-leg inverter and use it to compare the price of the inverters. We estimate the cost model of the main part of inverter based on the parameters that increase in proportion to the price of the parts sold on the market. An exchange rate of 1100 WON = 1 USD is applied because the price of the parts is sampled in Korean WON [31,32].

4.1. Cost Model of IGBT

The 3-leg inverter consists of six IGBTs and the 4-leg inverter has eight IGBTs. We derive the cost model from the 600 V product line, which is the rated voltage of the inverter, and the 1200 V product line with twice the voltage margin. To ensure the validity of the economic analysis, prices are compared using Microchip Technology's products with multiple samples for voltage ratings. Figure 17 shows the IGBT cost model with increasing current rating and is expressed as a log function of (8) and (9).

$$\tau_{\rm IGBT}^{600\rm V} = 102.9\,\ln x - 493.35\tag{8}$$

$$_{\rm IGBT}^{1200\rm V} = 84\ln x - 327.44 \tag{9}$$

where x is the current rating of IGBT.



Figure 17. Cost model of IGBT.

4.2. Cost Model of Capacitor

4.2.1. Cost Model of DC-Link Capacitor

The 3-leg inverter and 4-leg inverter have one electrolytic capacitor as a DC-link capacitor. Both inverters should analyze a product family of 600 V or higher, taking into account the voltage applied to the DC-link capacitor. However, due to the lack of samples of commercial products for high voltage electrolytic capacitors, prices are compared using TDK Electronics' 300 V, 400 V and 500 V product lines. A serial combination of capacitors can satisfy the working voltage and a parallel combination of capacitors can satisfy the required capacitance.

Figure 18 shows the cost model of an electrolytic capacitor. As the capacitance increases, the cost of the electrolytic capacitor increases linearly, as expressed in (10)–(12).

$$\sigma_{C_dc-link}^{300V} = 9.956x + 15.023 \tag{10}$$

$$\sigma_{C\ dc-link}^{400V} = 12.153x + 19.921 \tag{11}$$

$$\sigma_{C\ dc-link}^{500V} = 21.109x + 22.168\tag{12}$$

where x is the capacitance (mF) of the DC-link capacitor.

4.2.2. Cost Model of Filter Capacitor

The filter capacitor is analyzed based on the film capacitor. The rated voltage applied to the filter capacitor for both inverters is 380 V. Therefore, a cost model is generated by using the product line of 480 V, 550 V, and 780 V of KEMET considering voltage margin. As shown in Figure 19, the cost of increasing the capacitance of the film capacitor is linear, as expressed in (13)–(15).

$$\sigma_{C\ film}^{480V} = 0.1952x + 41.399\tag{13}$$

$$\sigma_{C\ film}^{455V} = 0.3902x + 39.721 \tag{14}$$

$$\sigma_{C\ film}^{780V} = 0.5346x + 51.968 \tag{15}$$

where x is the capacitance (μF) of the film capacitor.



Figure 18. Cost model of electrolytic capacitor.



Figure 19. Cost model of film capacitor.

4.3. Cost Model of Filter Inductor

The 3-leg inverter has three filter detectors, and the 4-leg inverter has three filter inductors and one neutral inductor. Unlike other parts, inductors do not have an appropriate distribution of products on the market. Therefore, we estimate the cost model from the sum of the price of core and wire. The core size and AWG of the wire required the design of the filter inductor with reference to [33] and the core cost model is shown in (16).

Figure 20a shows the core price per available magnetizing area (A_e) of TDK Electronics' toroidal core. As the A_e of the core increases, the price increases as an exponential function and is expressed in (16).

$$\sigma_{L,core}^{\text{Ae}} = 5.6424 \mathrm{e}^{0.007 \mathrm{x}} \tag{16}$$

where x means the A_e value of the core suitable for the filter inductor. Next, the AWG of the wire used in the filter inductor and the number of turns according to AL-value are considered [33]. When the number of turns of the inductor is determined, the wire diameter is calculated from (17). Here ρ_c is the electrical resistance of the copper wire, l_T is the mean-length per turn (MLT) of the windings, and P_{cu} is the amount of heat or energy wasted when the current flows.

$$d \ge \frac{2}{\sqrt{\pi}} I_S \sqrt{\frac{\rho_c l_T N}{P_{cu}}} \qquad \text{where, } N = \sqrt{\frac{L}{AL - value}} \tag{17}$$

To reduce skin effect and proximity effect losses in conductors, a copper-braid form, which is many thin wire strands individually insulated and twisted or woven together such as Litz wire, can be applied. However, since the wire price is calculated as part of the inductor price, we consider the AWG of a single wire for convenience.



Figure 20. Cost model of inductor: (a) Core price per available magnetizing area, Ae; (b) wire price according to AWG.

Figure 20b shows the price per meter per AWG of copper wire. As the wire thickens, the price per meter of the wire increases as an exponential function. The price per meter per AWG is given as (18).

$$\sigma_{L_wire} = 2.0277 e^{-0.23x}$$
(18)

4.4. Cost Comparison of the Inverter Using the Part Cost Model

In this section, the price of a 3-leg inverter and a 4-leg inverter are compared using the part cost model. The 3-leg requires six IGBTs and the 4-leg inverter needs eight IGBTs. An IGBT has 1200 V and 600 A ratings. The voltage applied to the DC-link capacitor of the two inverters is 600 V. To meet the working voltage, connect four 7.5 mF capacitors with a working voltage of 400 V in series parallel. Thus, the working voltage of the DC-link capacitor is 800 V and the capacitance is 15 mF. The applied voltage of the filter inductor is 380 V. It uses film capacitors with a voltage rating of 550 V and capacitance of 150 μ F with a voltage margin of about 1.5 times higher. In the case of inductors, the voltage applied

to the filter and the neutral inductor is the same, but the required inductance is different. Since the minimum size of the filter inductor core meeting the output power capacity is 131 mm, the design uses a T140 \times 103 \times 25 core of AL-value 1100 nH. We calculate the number of turns required for a filter inductor and a neutral inductor, derive the AWG and calculate the price of the wire by multiplying the price per meter of the wire with the turns and MLT (mean-length per turn).

The comparison of the 3-leg inverter and 4-leg inverter using the part cost model is shown in Figure 21. Comparing the price of two inverters with the design conditions of Table 1 results in a price difference of about USD 561. This is the result of the difference in the number of neutral inductors and the number of IGBTs. The price comparison in Figure 21 does not take into account all the parts, design and manufacturing costs of the inverter. A more accurate price comparison will be possible, considering that 4-leg inverters can increase program coding costs and increase additional design costs for controllers compared to 3-leg inverters.



Figure 21. Cost comparison of 3-leg and 4-leg inverters using the cost model of the part.

5. Conclusions

For 3-leg inverters and 4-leg inverters to which SVPWM control is applied, this paper analyzes the failure rate and MTBF based on a fault-tree and compares the price of the inverters. Because PCA is a reliability assessment that only takes into account the type, number and connection status of parts, the failure rate usually increases as the number of parts increases. However, the FTA results show a high failure rate in the order of split DC-link capacitor 3-leg inverter > 3-leg inverter > 4-leg inverter. In general, the 4-leg inverter with the largest number of parts should have the highest failure rate, but the redundancy effect significantly reduced the failure rate. For more accurate failure rate prediction, the failure rate and MTBF of the 4-leg inverter according to the lifecycle of the controller were analyzed. The MTBF of the controller shall be guaranteed for at least 10 years in order for the 4-leg inverter to secure MTBF of approximately eight years in the 25 °C operating conditions.

In conclusion, the 4-leg inverter has a price increase of USD 561 at the same power capacity compared to the 3-leg inverter, but reliability is greatly improved by enabling the operation of redundancy compensation while also enabling the adjustment of the energy flow or output voltage in unbalanced load conditions.

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References

- Douglass, P.J.; Trintis, I.; Munk-Nielsen, S. Voltage unbalance compensation with smart three-phase loads. In Proceedings of the Power Systems Computation Conference, PSCC 2016, Genoa, Italy, 20–24 June 2016; pp. 1–7.
- Hu, J.; Fu, X.; Liao, T.; Chen, X.; Ji, K.; Sheng, H.; Zhao, W. Low Voltage Distribution Network Line Loss Calculation Based on The Theory of Three-phase Unbalanced Load. In Proceedings of the 3rd International Conference on Intelligent Energy and Power Systems, IEPS 2017, Hangzhou, China, 10 October 2017; pp. 65–71.
- 3. Lin, F.; Tan, K.; Lai, Y.; Luo, W. Intelligent PV Power System with Unbalanced Current Compensation Using CFNN-AMF. *IEEE Trans. Power Electron.* **2019**, *34*, 8588–8598. [CrossRef]
- Han, J.; Oh, Y.S.; Gwon, G.H.; Kim, D.U.; Noh, C.H.; Jung, T.H.; Lee, S.J.; Kim, C.H. Modeling and Analysis of a Low-Voltage DC Distribution System. *Resources* 2015, 4, 713–735. [CrossRef]
- Wang, J.; Konikkara, D.D.; Monti, A. A generalized approach for harmonics and unbalanced current compensation through inverter interfaced distributed generator. In Proceedings of the IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems, PEDG 2014, Galway, Ireland, 24–27 June 2014; pp. 1–8.
- Bifaretti, S.; Lidozzi, A.; Solero, L.; Crescimbini, F. Comparison of modulation techniques for active split dc-bus three-phase four-leg inverters. In Proceedings of the IEEE Energy Conversion Congress and Exposition, ECCE 2014, Pittsburgh, PA, USA, 14–18 September 2014; pp. 14–18.
- Lin, Z.; Ruan, X.; Jia, L.; Zhao, W.; Liu, H.; Rao, P. Optimized Design of the Neutral Inductor and Filter Inductors in Three-Phase Four-Wire Inverter With Split DC-Link Capacitors. *IEEE Trans. Power Electron.* 2019, 34, 247–262. [CrossRef]
- 8. Liu, Z.; Liu, J.; Li, J. Modeling, Analysis, and Mitigation of Load Neutral Point Voltage for Three-Phase Four-Leg Inverter. *IEEE Trans. Ind. Electron.* 2013, 60, 2010–2021. [CrossRef]
- Hadidian Moghaddam, M.J.; Kalam, A.; Miveh, M.R.; Naderipour, A.; Gandoman, F.H.; Ghadimi, A.A.; Abdul-Malek, Z. Improved Voltage Unbalance and Harmonics Compensation Control Strategy for an Isolated Microgrid. *Energies* 2018, 11, 2688–2714. [CrossRef]
- Chee, S.J.; Kim, H.S.; Sul, S.K.; Ko, S. Common-Mode Voltage Reduction of Three-Level Four-Leg PWM Converter. *IEEE Trans. Ind. Appl.* 2015, 51, 4006–4016. [CrossRef]
- 11. Zhang, R.; Prasad, V.H.; Boroyevich, D.; Lee, F.C. Three-dimensional space vector modulation for four leg voltage source converters. *IEEE Trans. Power Electron.* 2002, 17, 314–326. [CrossRef]
- Aissani, M.; Aliouane, K. Three-dimensional space vector modulation for four-leg voltage-source converter used as an active compensator. In Proceedings of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM 2010, Pisa, Italy, 14–16 June 2010; pp. 1416–1421.

- Golwala, H.; Chudamani, R. New Three-Dimensional Space Vector-Based Switching Signal Generation Technique without Null Vectors and With Reduced Switching Losses for a Grid-Connected Four-Leg Inverter. *IEEE Trans. Power Electron.* 2016, *31*, 1026–1035. [CrossRef]
- Zhang, Q.; Zhang, P.; Zhao, S.; Gao, J.; Sun, X. Research on a discontinuous three-dimensional space vector modulation strategy for the three-phase four-leg inverter. In Proceedings of the IEEE 8th International Power Electronics and Motion Control Conference, IPEMC-ECCE Asia 2016, Hefei, China, 22–26 May 2016; pp. 575–580.
- 15. Llonch-Masachs, M.; Heredero-Peris, D.; Montesinos-Miracle, D.; Rull-Duran, J. Understanding the three and four-leg inverter Space Vector. In Proceedings of the 18th European Conference on Power Electronics and Applications, EPE ECCE Europe 2016, Karlsruhe, Germany, 5–9 September 2016; pp. 1–10.
- 16. Kim, J.H.; Sul, S.K. A carrier-based PWM method for three-phase four-leg voltage source converters. *IEEE Trans. Power Electron.* **2004**, *19*, 66–75. [CrossRef]
- 17. Kim, J.H.; Sul, S.K.; Kim, H.; Ji, J.K. A PWM strategy for four-leg voltage source converters and applications to a novel line interactive UPS in a three phase four wire system. In Proceedings of the 39th IEEE Industry Applications Conference, IAS 2004, Seattle, WA, USA, 3–7 October 2004; pp. 2202–2209.
- 18. Kim, S.Y.; Song, S.G.; Park, S.J. Minimum Loss Discontinuous Pulse-Width Modulation Per Phase Method for Three-Phase Four-Leg Inverter. *IEEE Access* 2020, *8*, 122923–122935. [CrossRef]
- 19. Gamini Jayasinghe, S.D.; Mahinda Vilathgamuwa, D.; Madawala, U.K. A Dual Inverter-Based Supercapacitor Direct Integration Scheme for Wind Energy Conversion Systems. *IEEE Trans. Ind. Appl.* **2013**, *49*, 1023–1030. [CrossRef]
- Reliability prediction of electric equipment. In *Rep. MIL-HDBK-217F*; Department of Defense, Washington DC, Tech.: Washington, DC, USA, 1991; Available online: http://everyspec.com/MIL-HDBK/MIL-HDBK-0200-0299/MIL-HDBK-217F_14591 (accessed on 3 January 2021).
- Choudhary, K.; Sidharthan, P. Reliability Prediction of Electronic Power Conditioner (EPC) using MIL-HDBK-217 based Parts Count Method. In Proceedings of the International Conference on Computer, Communication and Control, IC4 2015, Indore, India, 10–12 September 2015.
- Mou, H.; Hu, W.; Sun, Y.; Zhao, G. A Comparison and Case Studies of Electronic Product Reliability Prediction Methods Based on Handbooks. In Proceedings of the International Conference on Quality, Reliability, Risk, Maintenance, and Safety Engineering, QR2MSE 2013, Chengdu, China, 15–18 July 2013; pp. 112–115.
- 23. Jones, J.; Hayes, J. A comparison of electronic-reliability prediction models. IEEE Trans. Reliab. 1999, 48, 127–134. [CrossRef]
- 24. Yeo, S.C.; Kang, F.S. Fault-Tree Based Failure-Rate Analysis for Boost Converter and Interleaved Boost Converter. J. Electr. Eng. Technol. 2019, 14, 2375–2387. [CrossRef]
- 25. Kang, F.S.; Song, S.G. Fault-Tree Based Failure-Rate Analysis for Clamped-double Submodule employing dc-short current protecting function. *J. Electr. Eng. Technol.* **2020**, in press. [CrossRef]
- Khalil, M.; Soulatiantork, P. Reliability assessment of PV inverters. In Proceedings of the 14th IMEKO TC10 Workshop Technical Diagnostics, New Perspectives in Measurements, Tools and Techniques for System's Reliability, Maintainability and Safety 2016, Milan, Italy, 27–28 June 2016; pp. 389–393.
- 27. Shoults, L.W. Implementation of Design Failure Modes and Effects Analysis for Hybrid Vehicle Systems. Master's Thesis, Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, May 2016.
- 28. Basu, J.B. Failure Modes and Effects Analysis (FMEA) of a Rooftop PV System. Int. J. Sci. Eng. Res. 2015, 3, 51–55.
- 29. MIL-STD-1629A, Procedures for Performing a Failure Mode, Effects and Criticality Analysis, November 1980. Available online: https://www.fmea-fmeca.com/milstd1629.pdf (accessed on 3 January 2021).
- 30. IEC-60182, Analysis Techniques for System Reliability-Procedure for Failure Mode and Effects Analysis (FMEA). 2006. Available online: https://webstore.iec.ch/preview/info_iec60812%7Bed2.0%7Den_d.pdf (accessed on 3 January 2021).
- Burkart, R.; Kolar, J.W. Component cost models for multi-objective optimizations of switched-mode power converters. In Proceedings of the IEEE Energy Conversion Congress and Exposition ECCE 2013, Denver, CO, USA, 15–19 September 2013; pp. 2139–2146.
- 32. Domingues-Olavarría, G.; Fyhr, P.; Reinap, A.; Andersson, M.; Alaküla, M. From Chip to Converter: A Complete Cost Model for Power Electronics Converters. *IEEE Trans. Power Electron.* **2017**, *32*, 8681–8692. [CrossRef]
- 33. Valchev, V.C.; Bossche, A.V. Inductors and Transformers for Power Electronics, 1st ed.; CRC Press: Boca Raton, FL, USA, 2005; pp. 33-42.