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Carbon Nanotube Field Effect Transistor (CNTFET) and Resistive Random Access Memory (RRAM) Based Ternary Combinational Logic Circuits

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Abstract: The capability of multiple valued logic (MVL) circuits to achieve higher storage density when compared to that of existing binary circuits is highly impressive. Recently, MVL circuits have attracted significant attention for the design of digital systems. Carbon nanotube field effect transistors (CNTFETs) have shown great promise for design of MVL based circuits, due to the fact that the scalable threshold voltage of CNTFETs can be utilized easily for the multiple voltage designs. In addition, resistive random access memory (RRAM) is also a feasible option for the design of MVL circuits, owing to its multilevel cell capability that enables the storage of multiple resistance states within a single cell. In this manuscript, a design approach for ternary combinational logic circuits while using CNTFETs and RRAM is presented. The designs of ternary half adder, ternary half subtractor, ternary full adder, and ternary full subtractor are evaluated while using Synopsis HSPICE simulation software with standard 32 nm CNTFET technology under different operating conditions, including different supply voltages, output load variation, and different operating temperatures. Finally, the proposed designs are compared with the state-of-the-art ternary designs. Based on the obtained simulation results, the proposed designs show a significant reduction in the transistor count, decreased cell area, and lower power consumption. In addition, due to the participation of RRAM, the proposed designs have advantages in terms of non-volatility.

Keywords: multiple valued logic (MVL); resistive random access memory (RRAM); carbon nanotube field effect transistor (CNTFET); ternary logic systems; emerging technologies

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1. Introduction

Binary circuits for long been associated with the design of digital systems for performing computations on two possible logic values (0 or true and 1 or false) in the Boolean space. However, the binary integrated circuit design suffers from various critical issues such as complexity of the interconnects and the pin-out problems which limit the connections inside and outside of the circuit. Interconnects are the main source of power dissipation within a VLSI chip and they comprises 70% of total on-chip capacitance [1]. In integrated circuits, these interconnects occupy additional area, thereby causing several signal integrity issues such as noise and delay jitters. The implementation of energy efficient digital designs becomes quite challenging when scaling down the feature size into a nano-meter regime,

owing to reliability and performance issues. Moreover, many real-life applications, such as robotics and process control, face difficulties for systematic implementation only with the conventional binary logic [2]. To get over the limitations of binary logic, a logic system having more than two values that are associated with the logic levels, which is commonly referred to as the multiple valued logic (MVL), can be used for implementing digital system design. MVL is a very effective and practical means to resolve the issues of interconnects in modern circuits. Owing to the fact that the MVL utilizes more than two logic levels, MVL-based systems provide the transmission of a greater amount of information when compared to binary logic systems over a single wire, which helps to significantly reduce the on-chip and off-chip interconnections. The designs utilizing MVL for its implementation offer advantages in terms of increased information density, reduced chip area, and improved computational capability of the integrated circuits. Therefore, the use of MVL designs helps to reduce the circuit complexity and improve energy efficiency in digital system design due to reduced circuit overhead [3]. MVL is one of the new approaches, which increases the radix for computation to lower the complexity of the circuit. The main purpose of using MVL over binary logic is to: (i) reduce the chip area by the transmission of more information through each wire as compared to binary; (ii) increase the speed of information transmission as the information per unit time is increased; and, (iii) reduce the circuit complexity as each MVL element processes more information when compared to the binary element. The introduction of additional levels to the existing binary logic results in MVL systems, with typical examples being that of the ternary and quaternary logic systems [4]. Ternary logic is of considerable interest, due to its ease of implementation and energy efficiency because of the reduced complexity of interconnects and chip area [5]. In addition, ternary circuits can also help to reduce the problems of pin-out and increase in interconnection density in the VLSI systems.

MVL designs can replace the existing binary technologies due to its numerous advantages, but this is highly dependent on the circuit realization techniques that we employ for the implementation of MVL systems. A number of approaches to build MVL based circuit using CMOS or to combine binary and multi-valued blocks in logic circuits has been shown [6]. With the progress of nanotechnology, molecular devices are becoming promising alternatives to the traditional silicon-based CMOS technology [7]. The most promising alternative to silicon transistor for achieving low power and high performance is the Carbon nanotube field effect transistor (CNTFET) [8–10]. Carbon Nano Tubes (CNTs) have recently gained significant interest, primarily due to their relatively small dimensions and potential of implementation in many existing as well as emerging technologies. CNTFET could be the most suitable option for replacing conventional MOSFET based on silicon technology, because of its similarities in terms of various characteristics, such as near-ballistic transport operation due to its unique one-dimensional (1D) band structure, which gives the device an excellent driving capability and less power dissipation [11]. The threshold voltage of CNTFET can be controlled by varying the CNT diameter, which is very effective in the design of MVL based circuits. Additionally, CNTFETs (both p-type and n-type) have similar mobility values, which is quite significant for device sizing in complex circuits. However, CNTFETs face some critical challenges in terms of chirality control, fabrication process, growth, and the positioning of single-wall CNTs.

Ternary systems can also be implemented while using another suitable emerging technology, commonly referred to as the Resistive Random Access Memory (RRAM). This is attributed to the fact that the RRAM device can effectively implement multiple logic values (two or more) without the need for extra hardware for the realization of digital designs. Thus, the implementation of ternary logic while utilizing RRAM, provides a unique opportunity for enhanced and novel functionality. The circuit schematic of RRAM is quite simple, having a two terminal metal-insulator-metal (MIM) structure, with the external voltage pulse causing a resistance change within the device [12,13]. Its physical mechanism relies on the formation and annihilation of a conductive filament (CF) in the oxide (dielectric) connecting the two metal electrodes [14,15]. This resistance shift between

the high resistance state (HRS) and low resistance state (LRS) is effectively used for data storage in the form of "0" and "1" [16–18], respectively. Because of the various attractive features of RRAM, such as higher on/off ratio, non-volatility, good scalability, and low ON-state resistance [19,20], it is employed for configuring logic gates, including the field-programmable gate arrays [21] that are used in the design of digital systems. The RRAM is chosen as the candidate device here, as it has a simple structure, enables high integration density, and it can exhibit switching in the low-power regime [22]. Although making use of RRAM for implementing ternary logic systems is still in its emerging phase, various methodologies for the implementation of binary logic gates with RRAM have already been proposed [23] .

The main aim of this paper is to utilize CNTFET-RRAM ternary logic gates for the design of ternary arithmetic circuits in order to explore the advantages in terms of reduction of gate count by utilizing the negation of literals technique. In this manuscript, CNTFET-RRAM ternary combinational logic circuits are proposed and the simulation results while using the HSPICE simulator demonstrates advantages in terms of power consumption and component count when compared to the multi-valued logic designs existing in the literature. Logic states can also be stored in the RRAM due to the addition of RRAM as circuit element. This will ensure the integration of logic computation and data storage into the proposed designs, which opens a new domain of opportunities for exploring intelligent computation systems.

The rest of the paper is presented, as below. Section 2 provides a brief introduction of the carbon nanotube transistors. In Section 3, an overview of ternary logic is presented and the design methodology for various ternary combinational logic circuits is detailed. The simulation results that were obtained from HSPICE software and the comparative analysis are described in Section 4. Finally, Section 5 concludes the paper.

2. Carbon Nanotube Field Effect Transistors

Carbon Nanotubes (CNTs) came into existence in 1991 and the credit for its discovery was given to a Japanese physicist, S. lijima [24]. CNT is a nanoscale tube that is made up of rolled sheets of graphene and it can be either single-walled (SWCNT) or multi-walled (MWCNT). SWCNT consists of a single nanotube, whereas MWCNT is made up of multiple nanotubes with interlayer spacing of 0.34 nm. SWCNTs exhibit various properties, such as quasi ballistic carrier transport and suppression of short channel effects because of the one-dimensional electron transport [25]. SWCNT can act as either a conductor or a semiconductor, depending upon the angle of atom arrangement along the CNT, and it is represented by an integer pair (n, m), called chirality vector. In addition, SWCNTs can be either semiconducting or metallic in nature, depending upon the indices (n, m), which specify the nature of carbon atoms along the tube [26]. The nanotube is metallic if n = m or n − m = 3i, where "i" is an integer; otherwise, the nanotube is semiconducting.

Figure 1 shows the schematic of CNTFET having SWCNT placed between the two electrodes. From the figure, we observe that the highly doped CNTs are placed between the gate and the source/drain electrodes. These heavily doped CNT segments offer low electrical resistance in the ON-state of the CNTFET. The undoped CNTs that are placed under the gate electrode serve as the channel. The CNTFET gate width can be obtained from Equation (1) as [27].

$$W_{gate} \approx Max(W_{min}, M \times P) \quad (1)$$

where M represents tube number of CNT, W_{min} is the minimum value of gate width, and P is the pitch value, referring to the distance between two adjacent CNTs.

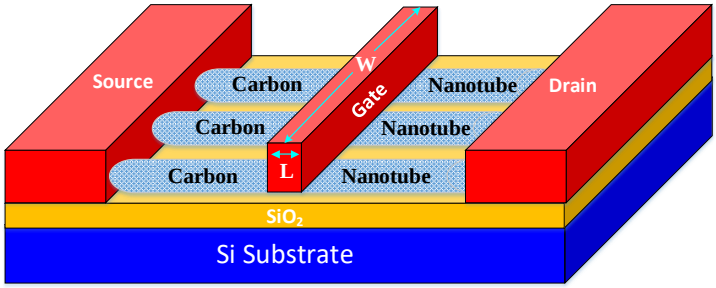


Figure 1. Schematic of a Carbon Nanotube Field Effect Transistor (CNTFET).

In order to calculate the diameter of the CNT, we make use of Equation (2) as [28].

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{n^2 + m^2 + nm} \tag{2}$$

where a_0 = 0.142 nm is the distance between the neighbouring carbon atoms and n, m are the chirality vectors that specify the roll orientation of CNT. Therefore, Equation for D_{CNT} in nanometers can be rewritten as Equation (3).

$$D_{CNT} = 0.0783\sqrt{n^2 + m^2 + nm} \tag{3}$$

Similar to the traditional MOSFET, CNTFET has four terminals. The channel region of the device consists of undoped nanotubes, which are semiconducting in nature and are placed in the channel region beneath the gate, while the nanotubes that are highly doped, and the placement is between the source/drain terminals and the gate. The device can then be turned either on or off, depending on the potential applied to the gate. The threshold voltage of CNTFET [28] is expressed in Equation (4), as.

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{a}{e}\frac{V_\pi}{D_{CNT}} \approx \frac{0.436}{D_{CNT}} \tag{4}$$

where e is the electron charge, E_g represents bandgap, a = 2.49 Å is the carbon atom distance, and V_π = 3.033 eV is the carbon π-π bond energy in the tight bonding model.

From Equations (3) and (4), we observe that the threshold voltage of the CNTFET is controlled by the diameter of the CNT, which, in turn, depends upon the the chirality vector (n, m). Thus, by changing the chirality vector or the diameter of the CNT, it is possible to control the threshold voltage of CNTFET [29]. Figure 2a shows the threshold voltage of both p-type CNTFET and n-type CNTFET obtained from Equation (4), and HSPICE simulation for various chirality vectors (various n for m = 0). The threshold voltage distribution of n-type CNTFET is the same as the P-type CNTFET, but with opposite sign. CNTFETs provide a unique opportunity to control threshold voltage by changing the chirality vector, or the diameter of the CNT [5].

Figure 2 depicts the characteristics current-voltage curve of an n-type MOSFET in 32 nm technology and a n-type CNTFET in 32 nm technology. From Figure 2b, we observe that the I_D-V_{DS} characteristics of 32 nm CNTFET are more desirable when compared to that of a 32 nm MOSFET. In addition, from Figure 2c, we observe that the I_D-V_{GS} curve of CNTFET is quadratic in saturation region, as compared to the linear I_D-V_{GS} characteristics of MOSFET. This signifies that CNTFET has a higher transconductance (g_m) in comparison to that of MOSFET.

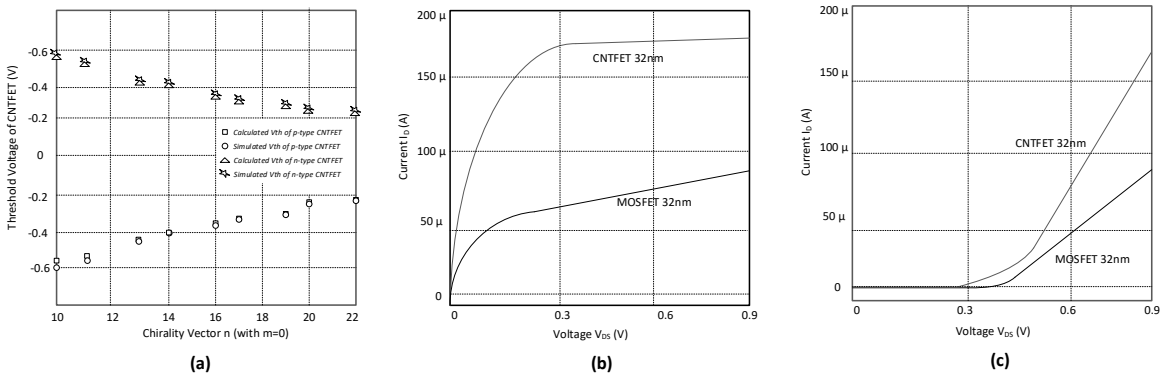


Figure 2. (**a**) CNTFET threshold variation with varying n (for m = 0). (**b**) Comparison of I–V curve of n-type MOSFET with n-type CNTFET in 32 nm technology for I_D-V_{DS}. (**c**) Linear scale I_D-V_{GS} .

3. Circuit Level Implementation of Ternary Logic

For an existing binary system, voltage levels 0 V and V_{dd} are represented by two logic values '0' and '1', respectively. For the case of ternary systems, voltage levels 0 V, $\frac{V_{dd}}{2}$, and V_{dd} represent logic values '0', '1', and '2', respectively.

By utilizing ternary logic in design of digital systems, energy efficiency and simplicity can be achieved due to the reduced interconnect complexity as well as the chip area [30], therefore resulting in smaller power delay [31]. In addition, the transmission channels can be better utilized due to the higher storage density of each line. Additionally, the serial and serial-parallel arithmetic operations can be carried out faster by employing ternary logic. The numbers are represented in MVL systems in a balanced mode representation and unbalanced mode representation. However, the balanced mode representation is not used quite often, as it becomes difficult to deal with the negative voltages.

Let us assume that ternary values to represent false, undefined, and true conditions are 0, 1, and 2, respectively. Any ternary function of n variables (A_1, A_2 . . . A_n) is defined as a logic function mapping from $\{0,1,2\}^n$ to {0, 1, 2}. The fundamental ternary logic operations are defined in Equation (5), as [32].

$$\begin{aligned} \overline{A_i} &= 2 - A_i \\ A_i \bullet A_j &= min\{A_1, A_2\} \\ A_i + A_j &= max\{A_1, A_2\} \end{aligned} \tag{5}$$

where A_i, A_j ε $\{0,1,2\}$, and '-' represent the arithmetic subtraction. '$\overline{A_i}$' refers to the logical NOT operation, whereas '$A_i \bullet A_j$' and '$A_i + A_j$' represent logical AND and logical OR operations, respectively. Table 1 shows the logic symbols that we assume for ternary logic design.

Table 1. Logic Symbols.

Voltage Level	Logic Value
0	0 (Low)
$\frac{V_{dd}}{2}$	1 (Intermediate)
V_{dd}	2 (High)

In ternary logic, there exist 3^{3^n} modal functions and 3^n combinations, where n is a variable. When n = 1, we have one-variable functions *f(y)*, and there are 3^{3^1} = 27 modal functions, called Literals. If n = 2, there are 3^{3^2} = 19,683 two variable functions. Literal is denoted by Y_i^a, where a^i = 0, 1, 2, 01, 02 and 12 defined in Equations (6)–(13) as [33].

$$Y_i = \begin{cases} 0, & \text{if Y} \neq \text{i} \\ 2, & \text{if Y = i} \quad \text{where i = 0,1,2.} \end{cases} \tag{6}$$

$$Y_{01} = Y_0 + Y_1 \tag{7}$$

$$Y_{12} = Y_1 + Y_2 \tag{8}$$

$$Y_{02} = Y_0 + Y_2 \tag{9}$$

$$Y_{01} \bullet Y_{12} = Y_1 \tag{10}$$

$$Y_{01} \bullet Y_{02} = Y_0 \tag{11}$$

$$Y_{02} \bullet Y_{12} = Y_2 \tag{12}$$

$$Y_0 + Y_1 + Y_2 = 2 \tag{13}$$

This paper focuses on utilizing CNTFET-RRAM ternary logic gates, a modified level shifter circuit and negation of literals technique in order to reduce the number of devices required for representing combinational logic functions. In addition, the negation of literals (Y_i) that is given by Equations (14)–(18) is quite useful in reducing the number of ternary gates.

$$NEG(Y_i) = \begin{cases} 0, & \text{if Y = i} \\ 2, & \text{if Y} \neq \text{i} \end{cases} \tag{14}$$

$$Y_2 = \overline{Y_{01}} \quad \& \quad Y_{01} = \overline{Y_2} \tag{15}$$

$$Y_1 = \overline{Y_{02}} \quad \& \quad Y_{02} = \overline{Y_1} \tag{16}$$

$$Y_0 = \overline{Y_{12}} \quad \& \quad Y_{12} = \overline{Y_0} \tag{17}$$

$$\overline{0} = 2 \quad \overline{2} = 0 \tag{18}$$

3.1. Overview of CNTFET-RRAM Ternary Logic Gates

Ternary logic gates that are designed using CNTFET-RRAM show improved performance in terms of lower power consumption, as the use of large resistors in the circuit is avoided, which resulted in higher power dissipation. For the design of digital systems, the basic gates are inverters, and the universal gates, i.e., NAND gates and NOR gates. Figure 3 depicts the logic symbols used for representing the basic ternary logic gates (Standard ternary inverter (STI), positive ternary inverter (PTI), negative ternary inverter (NTI), TNAND, and TNOR). Ternary inverters are classified, as: standard ternary inverter (STI), positive ternary inverter (PTI), and negative ternary inverter (NTI). For STI, three different logic levels (0, 1, and 2) are used in order to represent ternary numbers; whereas, for the case of PTI and NTI, we have only two logic levels (0 and 2) at the output corresponding to the three different logic levels at the input [33]. The STI, PTI, and NTI functions are given by Equations (19)–(21), as.

$$Y_{STI} = f_0(x) = 2 - x \tag{19}$$

$$Y_{PTI} = f_1(x) = \begin{cases} 2, & \text{if } x \neq 2 \\ 0, & \text{if } x = 2 \end{cases} \tag{20}$$

$$Y_{NTI} = f_2(x) = \begin{cases} 2, & \text{if } x = 0 \\ 0, & \text{if } x \neq 0 \end{cases} \tag{21}$$

For the case of ternary NAND and ternary NOR, the outputs for the inputs X_1 and X_2 are given by Equations (22) and (23), respectively.

$$Y_{NAND} = \overline{min\{X_1, X_2\}} \tag{22}$$

$$Y_{NOR} = \overline{max\{X_1, X_2\}} \quad (23)$$

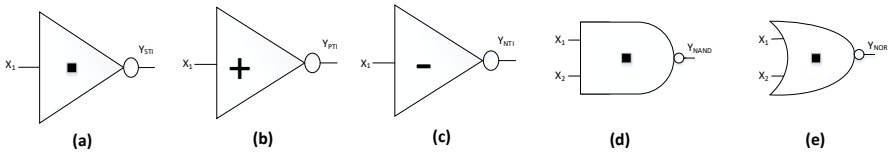


Figure 3. Symbols of Ternary Logic Gates: (**a**) Standard ternary inverter (STI); (**b**) positive ternary inverter (PTI); (**c**) negative ternary inverter (NTI); (**d**) TNAND; and, (**e**) TNOR [17].

Figure 4a shows the circuit structure of CNTFET-RRAM based STI (Standard Ternary Inverter) previously described in [17]. The circuit is composed of two CNTFETs (N_1, N_3), p-type CNTFET (with gate connected to the ground), (N_2) and RRAM device (X_1). The CNTs N_1, N_2, and N_3 have chirality (19, 0), (10, 0), and (19, 0), respectively. From Equation (2), the diameters of N_1, N_2, and N_3 are 1.487 nm, 0.783 nm, and 1.487 nm, respectively. Therefore, from Equation (4), the threshold voltages of N_1, N_2, and N_3 are 0.293 V, -0.557 V, and -0.293 V, respectively. The number of tubes used for N_1 and N_2 is 3, while for N_2 is 1.

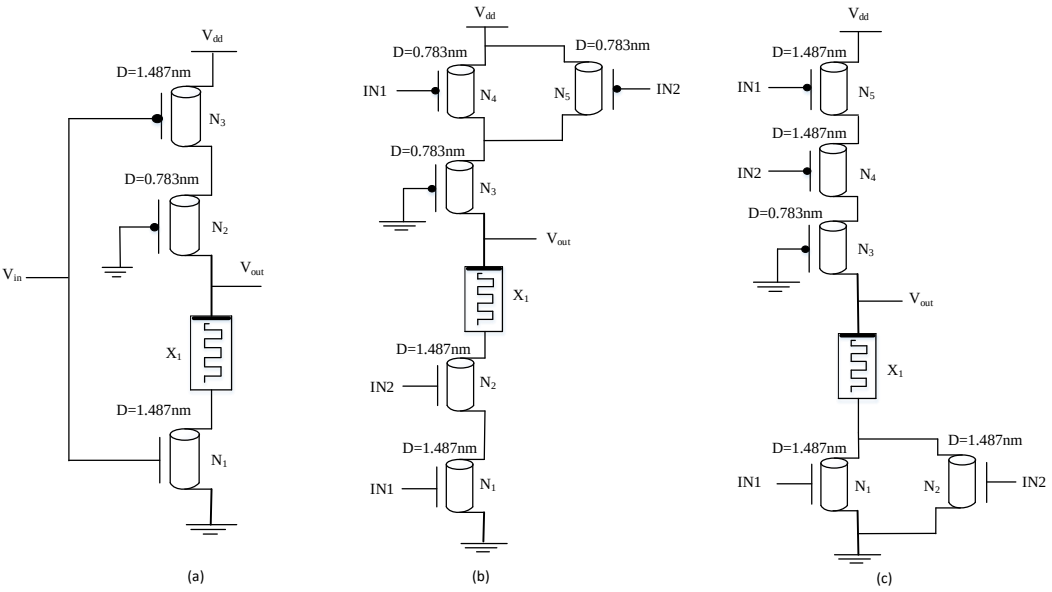


Figure 4. Schematic of (**a**) STI; (**b**) Ternary NAND; and, (**c**) Ternary NOR [17].

The noise margin of the STI is determined graphically by plotting the voltage transfer curve of the ternary inverter. The VTC of the CNTFET-RRAM based STI is depicted in Figure 5. In ternary logic, four noise margins (NM_H, NM_{MH}, NM_{ML}, NM_L) are specified for four voltage points (V_{IH}, V_{IMH}, V_{IML}, V_{IL}), as shown in the VTC curve. The static noise margin (SNM) of the STI is the smallest one among the four noise margins (NM_H, NM_{MH}, NM_{ML}, NM_L). Table 2 presents the benchmarking of the proposed and the existing STI designs regarding the SNM.

Table 2. Noise Margin values for STI designs.

Parameter	Mahmood et al. [34]	Proposed STI
NM_H (mV)	159	70
NM_{MH} (mV)	140	100
NM_{ML} (mV)	141	120
NM_L (mV)	154	150
SNM (mV)	140	100

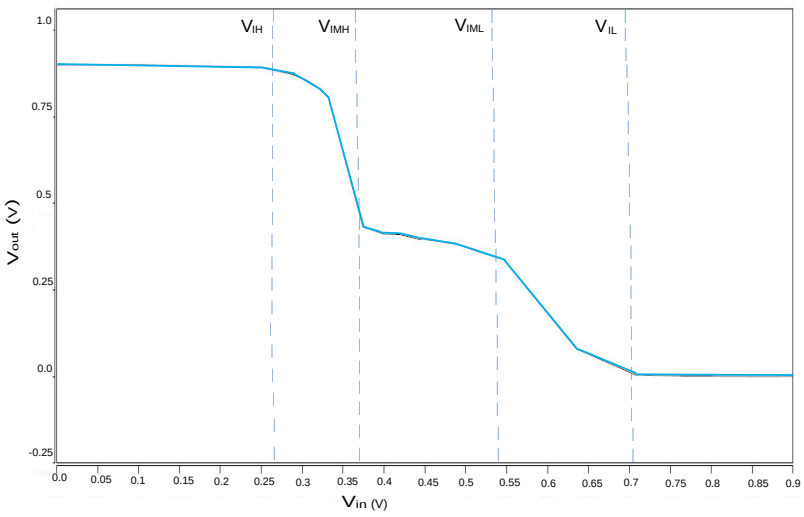


Figure 5. Voltage transfer curve (VTC) of Standard ternary inverter (STI) circuit.

CNTFET-RRAM ternary NAND and NOR gate schematic is depicted in Figure 4b,c, respectively. CNT chirality used in N_1, N_2, N_4, N_5 is (19, 0) while for N_3 is (10, 0) for both the ternary NAND and NOR gates. The number of tubes used for N_1, N_2, N_4, and N_5 is three while, for N_3, is one.

The existing CNTFET-RRAM ternary gates can be implemented for the design of various arithmetic and combinational ternary logic designs. Despite significant progress, CNTFETs were until recently fabricated only in academic or research laboratories. However, a standard solution-based method that significantly improves the throughput, while simultaneously reducing the cost has been discovered, which allows for fabricating CNTFETs in a commercial silicon manufacturing facility with industry standard 200 mm wafers, employing the same equipment that is currently being used to fabricate silicon product wafers. Two different industry manufacturing facilities have reported successful fabrication of CNTFETs (i) a commercial silicon manufacturing facility (Analog Devices, Inc., Norwood, MA, USA, with more than 43,000 different products in production) and (ii) a high-volume manufacturing semiconductor foundry (Sky Water Technology, a US-based semiconductor foundry with more than 12,000 wafer starts per month capacity). The CNTFETs were fabricated while using the same equipment currently being used to fabricate silicon product wafers, explicitly demonstrating that CNTFET fabrication is Silicon-CMOS-compatible [35]. On the other hand, RRAM devices are CMOS-compatible and they can be fabricated with the existing state-of-the-art technology without the need of special equipment and materials. Thus, RRAM and CNTFETs can be built while using the traditional silicon-chip fabrication, which makes their integration feasible, thus making our designs more practically realizable.

3.2. Ternary Decoder

The ternary decoder that is depicted in Figure 6 is a combinational logic circuit having a single input and three outputs that are represented by Equation (24) as [17]:

$$A_n = \begin{cases} 2, & \text{if A = n} \\ 0, & \text{if A} \neq \text{n} \end{cases} \tag{24}$$

where n can have 0, 1, or 2 logic values. The decoder functions, as follows: if the input is 0, A_0 equals 2. If the input is 2, A_2 equals 2, and, if the input is 1, NOR gate makes A_1 = 2, because A_0 and A_2 are zero.

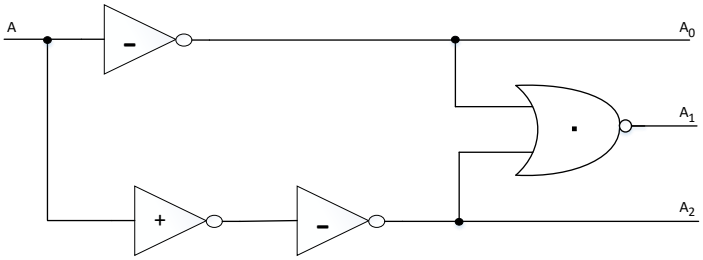


Figure 6. Schematic of Ternary Decoder.

3.3. Ternary Half Adder

A ternary half adder is a combinational logic circuit that is depicted in Figure 7 that performs the addition of two bits and produces outputs sum and carry based on Equation (25) as [17].

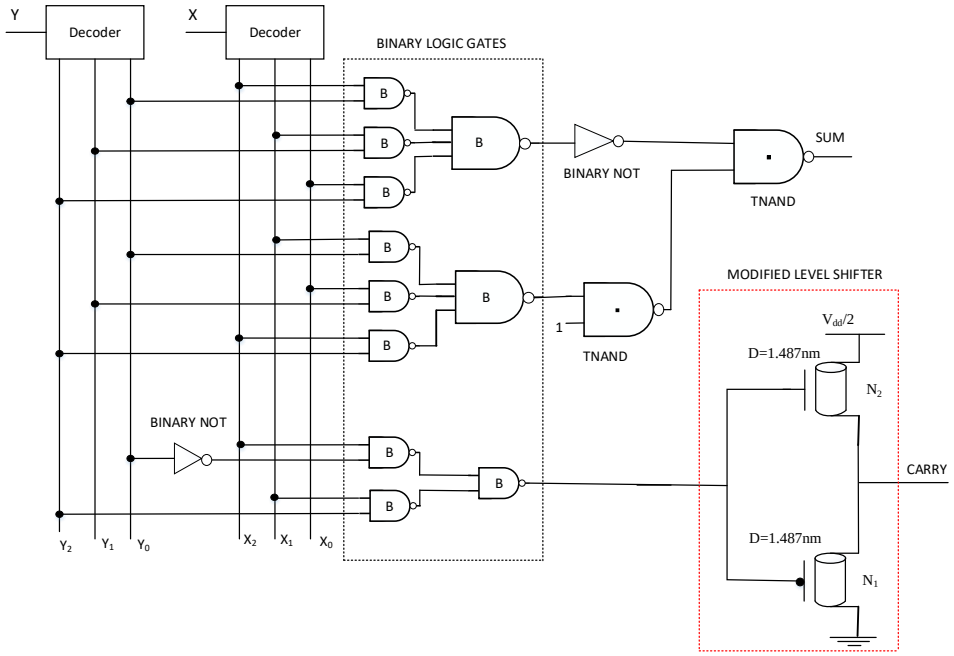


Figure 7. Schematic of Ternary Half Adder.

$$\begin{aligned} SUM &= X_0Y_2 + X_1Y_1 + X_2Y_0 = 1.(X_0Y_1 + X_1Y_0 + X_2Y_2) \\ CARRY &= 1.(X_2Y_1 + X_1Y_2 + X_2Y_2) \\ CARRY &= 1.(X_2[Y_1 + Y_2] + X_1Y_2) \end{aligned} \tag{25}$$

The equation for CARRY due to the negation of literals [33] is given in (26), as.

$$CARRY = 1.(X_2Y_{12} + X_1Y_2) = 1.(X_2\overline{Y_0} + X_1Y_2) \tag{26}$$

where X_n and Y_n are the outputs of the ternary decoder to the inputs X and Y, respectively. The SUM and CARRY functions that are specified in Equations (25) and (26) are implemented while using the binary gates along with the CNTFET-RRAM ternary gates.

A modified level shifter (LS) circuit that is shown in Figure 7 is implemented in order to obtain a logic function as:

$$Out = \begin{cases} 1, & \text{if in} = 1,2 \\ 0, & \text{if in} = 0 \end{cases} \quad (27)$$

3.4. Ternary Half Subtractor

A ternary half subtractor that is shown in Figure 8 is a combinational circuit that subtracts one bit from the other and generates DIFFERENCE and BORROW outputs, which are based on Equation (28), as [17].

$$DIFFERENCE = X_0Y_1 + X_1Y_2 + X_2Y_0 = 1.(X_1Y_0 + X_2Y_1 + X_0Y_2)$$
$$BORROW = 1.(X_0Y_1 + X_0Y_2 + X_1Y_2)$$
$$BORROW = 1.(X_0[Y_1 + Y_2] + X_1Y_2) \quad (28)$$

The equation for BORROW due to the negation of literals [33] is given in (29), as.

$$BORROW = 1.(X_0Y_{12} + X_1Y_2) = 1.(X_0\overline{Y_0} + X_1Y_2) \quad (29)$$

where X_n and Y_n are the outputs of the ternary decoder to the inputs X and Y, respectively. In this case, similar to the ternary half adder, the decoders X and Y generate the output signals, whereas the DIFFERENCE and BORROW functions that are specified in (28) and (29) are implemented using binary gates along with the CNTFET-RRAM ternary gates.

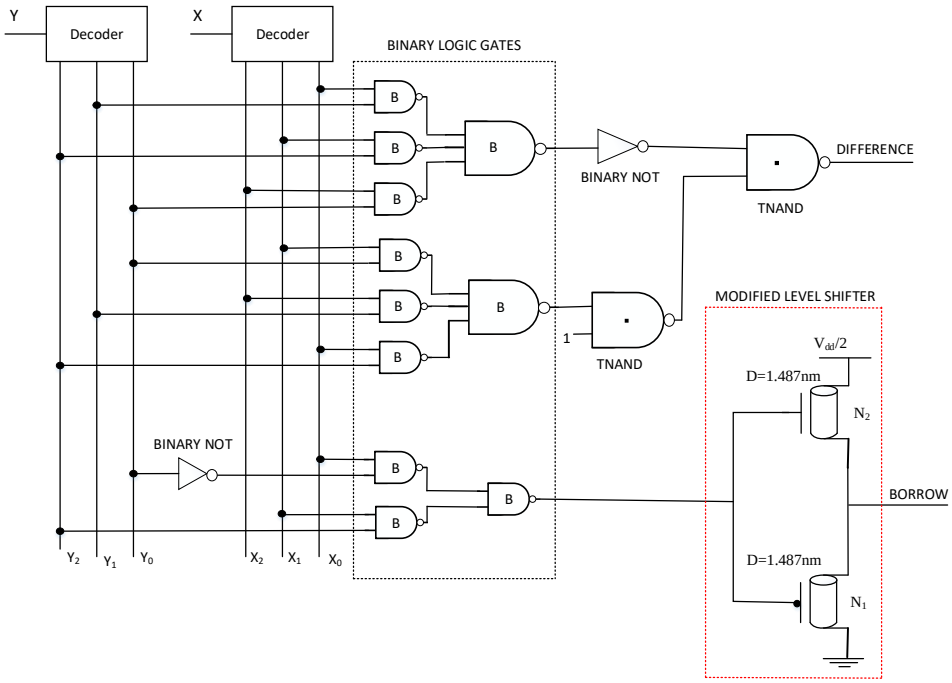


Figure 8. Schematic of Ternary Half Subtractor.

3.5. Ternary Full Adder

A ternary full adder circuit that is depicted in Figure 9 is a combinational logic circuit that is implemented while using ternary decoders, binary, and ternary logic gates. The circuit has inputs X, Y, Z and it produces SUM and CARRY outputs that are based on Equations (30) and (31).

$$SUM = Z_0[X_2Y_0 + X_1Y_1 + X_0Y_2] + Z_1[X_1Y_0 + X_0Y_1 + X_2Y_2] + Z_2[X_0Y_0 + X_2Y_1 + X_1Y_2] + 1.\{Z_0[X_1Y_0 + X_0Y_1 + X_2Y_2]Z_1[X_0Y_0 + X_2Y_1 + X_1Y_2] + Z_2[X_2Y_0 + X_1Y_1 + X_0Y_2]\} \quad (30)$$

$$CARRY = X_2Y_2Z_2 + 1.\{Z_0[X_1Y_2 + X_2Y_1 + X_2Y_2] + Z_1[X_1Y_1 + X_2 + Y_2] + Z_2[X_1 + X_2 + Y_1 + Y_2]\} \quad (31)$$

The equation for CARRY due to the negation of literals [33] is given in (32), as.

$$\begin{aligned} CARRY &= X_2Y_2Z_2 + 1.\{X_{12}Y_2Z_0 + X_2Y_1Z_0 + X_1Y_1Z_1 + X_2Z_{12} + X_1Z_2 + Y_1Z_2\} \\ &= X_2Y_2Z_2 + 1.\{\overline{X_0}Y_2Z_0 + X_2Y_1Z_0 + X_1Y_1Z_1 + X_2\overline{Z_0} + Y_2\overline{Z_0} + X_1Z_2 + Y_1Z_2\} \end{aligned} \quad (32)$$

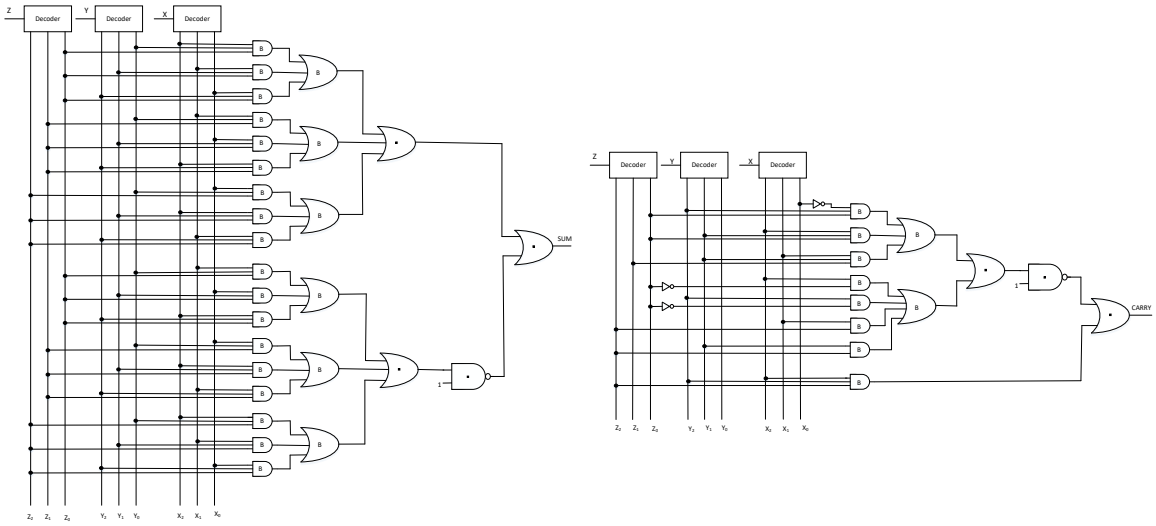


Figure 9. Schematic of Ternary Full Adder.

3.6. Ternary Full Subtractor

A ternary full subtractor circuit that is depicted in Figure 10 is a combinational logic circuit, which is implemented while using ternary decoders, binary, and ternary logic gates. The circuit has inputs X, Y, Z and it produces DIFFERENCE and BORROW outputs based on Equations (33) and (34).

$$DIFFERENCE = X_0Y_0Z_1 + X_0Y_1Z_0 + X_2Y_2Z_0 + X_1Y_0Z_2 + X_1Y_1Z_1 + X_1Y_2Z_0 + X_2Y_0Z_0 + X_2Y_1Z_2 + X_2Y_2Z_1 + 1.\{X_0Y_0Z_2 + X_0Y_1Z_1 + X_2Y_2Z_1 + X_1Y_0Z_0 + X_1Y_1Z_2 + X_1Y_2Z_1 + X_2Y_0Z_1 + X_2Y_1Z_0 + X_2Y_2Z_2\} \quad (33)$$

$$BORROW = X_0Y_2Z_2 + 1.\{X_0Z_2 + X_1Z_2 + X_0Z_1 + X_0Y_2 + X_1Y_2 + X_2Y_1 + Y_2Z_1 + Y_2Z_2 + Y_1Z_2 + X_0Y_1Z_0 + X_1Y_1Z_1\} \quad (34)$$

The equation for BORROW due to the negation of literals [33] is given in (35), as.

$$\begin{aligned} BORROW &= X_0Y_2Z_2 + 1.\{X_{01}Z_2 + X_0Z_1 + X_{01}Y_2 + Y_2Z_{12} + Y_1Z_2 + X_0Y_1Z_0 + X_1Y_1Z_1\} \\ &= X_0Y_2Z_2 + 1.\{\overline{X_2}Z_2 + X_0Z_1 + \overline{X_2}Y_2 + Y_2\overline{Z_0} + Y_1Z_2 + X_0Y_1Z_0 + X_1Y_1Z_1\} \end{aligned} \quad (35)$$

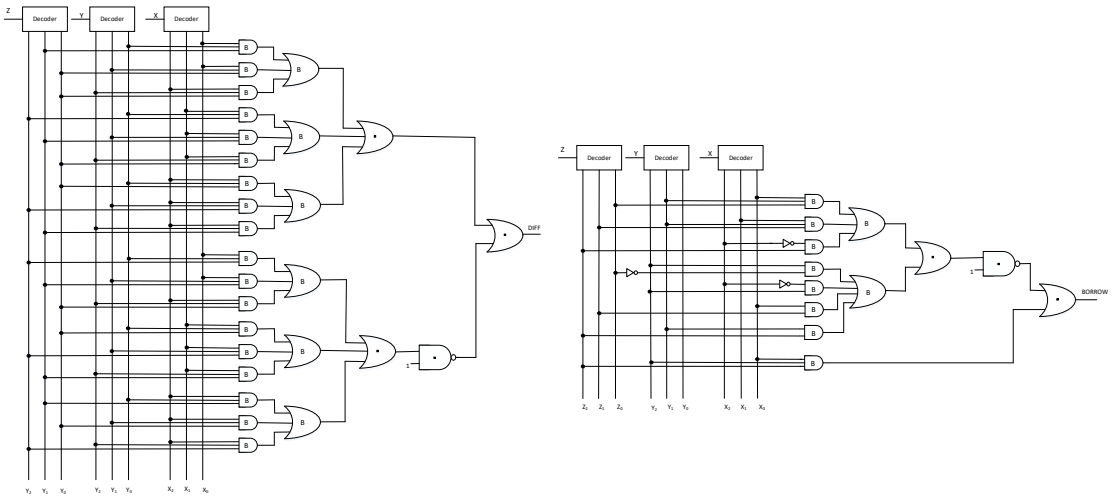


Figure 10. Schematic of Ternary Full Subtractor.

4. Results and Discussion

For simulation, 32-nanometre technology node, 0.9 V supply voltage at room temperature for all ternary designs is considered. The Stanford University CNTFET model [36] is implemented for analysis of all the designs in order to validate the operational performance. The Stanford model is SPICE compatible with channels that are composed of semiconducting single-walled carbon nanotubes having chirality that is user-specified and has channel length scaling effects that can be modelled down accurately to 20 nm. Table 3 lists the parameters of the CNTFET model and their values employed in the design. For RRAM, the Stanford University RRAM model [37] is employed. This RRAM model is physics-based spice compatible model that illustrates the switching performance of RRAM. This model is based on the growth of conductive filament (CF) and it includes the effect of critical phenomenon of switching, such as Joule heating and temperature change. The CF leaves a gap with the top electrode, which is called the filament gap. Thus, the rate of filament growth and filament gap govern the dynamics of this model. Table 4 provides a brief description of the RRAM parameters.

Table 3. Characteristic parameters and their values employed for the Stanford University CNTFET model.

Parameter of CNTFET	Specification of Parameter	Value
L_{ch}	Length of the physical channel	32 nm
L_{geff}	Mean free path length of intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
T_{ox}	Thickness of the top gate dielectric material	4 nm
EFI	The Fermi level of the doped S/D tube	6 ev
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
C_{sub}	Coupling capacitance along the substrate and the channel	20 pF/m

Table 4. Characteristic parameters of Stanford University Resistive Random Access Memory (RRAM) model.

Parameter	Parameter Description	Value
T_ini	Initial Device Temperature	298 K
F_min	Minimum field to enhance gap formation	1.4×10^9 V/m
t_{ox}	Oxide thickness	12 nm
gap_ini	Initial gap distance	1.8 nm
gap_min	minimum gap distance	0.2 nm
gap_max	maximum gap distance	1.8 nm
E_a	Activation energy for vacancy generation	0.6 eV

4.1. Functional Validation

The ternary circuits (half adder, half subtractor, full adder, and full subtractor) simulation is performed using HSPICE software. By utilizing the negation of literals technique, and the modified level shifter circuit, the proposed CNTFET-RRAM ternary combinational logic circuits achieve significant power savings. This is primarily due to the reduced component count as compared to the existing designs, which also results in a reduced area of the proposed circuits. For delay measurements, the delay values for all transitions are taken into account, and the average of the measurements is recorded as the average delay. In order to evaluate the power delay product (PDP), the power consumption and the average delay are multiplied. Table 5 lists the values that were obtained for power consumption, average delay, and power delay product obtained from HSPICE simulations.

Figure 11 depicts the input and output waveforms for the proposed ternary half adder utilizing CNTFET-RRAM ternary logic gates. From the simulations performed using SPICE software, the power consumption and the delay are computed as 0.0034 µW and 25.11 ns, respectively. Therefore, the power delay product is computed to 0.085 fJ.

Figure 12 depicts the input and the output waveforms for the proposed ternary half subtractor utilizing CNTFET-RRAM ternary logic gates. From the simulations that were performed using SPICE software, the power consumption and the delay are computed as 0.00102 µW and 0.874 ns, respectively. Therefore, the power delay product is computed to 0.00089 fJ.

Figure 13 depicts the input and the output waveforms for the proposed ternary full adder utilizing CNTFET-RRAM ternary logic gates. From the simulations performed using SPICE software, the power consumption and the delay are computed as 19.6 µW and 0.782 ns, respectively. Therefore, the power delay product is computed to 15.327 fJ.

The input and the output waveforms for the proposed ternary full subtractor utilizing CNTFET-RRAM ternary logic gates is depicted in Figure 14. From the simulations performed using SPICE software, the power consumption and the delay are computed as 20.10 µW and 0.7079 ns, respectively. Therefore, the power delay product is computed as 14.228 fJ.

Table 5. Power Consumption, Delay, and Power Delay Product comparison for the ternary combinational logic circuits.

DESIGN	Power Consumption (μW)	Average Delay (nS)	Power Delay Product(PDP) (fJ)
Ternary Half Adder			
Samadhi et al. [28]	2.221	0.0999	0.221
Lin et al. [32]	4.01	0.1101	0.4411
Sridevi et al. [33]	0.77	0.0052	0.0041
Shahrom et al. [38]	0.17	0.016	0.0027
Proposed	0.0034	25.11	0.085
Ternary Half Subtractor			
Sridevi et al. [33]	0.99	0.0071	0.00702
Proposed	0.00102	0.874	0.00089
Ternary Full Adder			
Sridevi et al. [33]	1.06	0.0096	0.0102
Das et al. [39]	0.24	6.2	1.488
Navi et al. [40]	1.05	0.0783	0.0822
Navi et al. [41]	0.783	0.0536	0.042
Proposed	19.6	0.782	15.327
Ternary Full Subtractor			
Sridevi et al. [33]	0.88	0.0177	0.0155
Proposed	20.10	0.7079	14.228

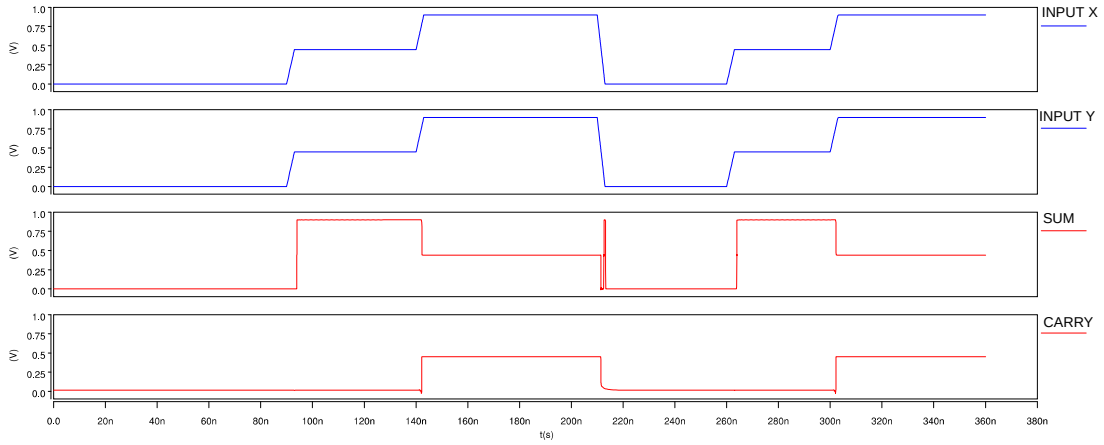


Figure 11. Input and Output waveforms of Ternary Half Adder.

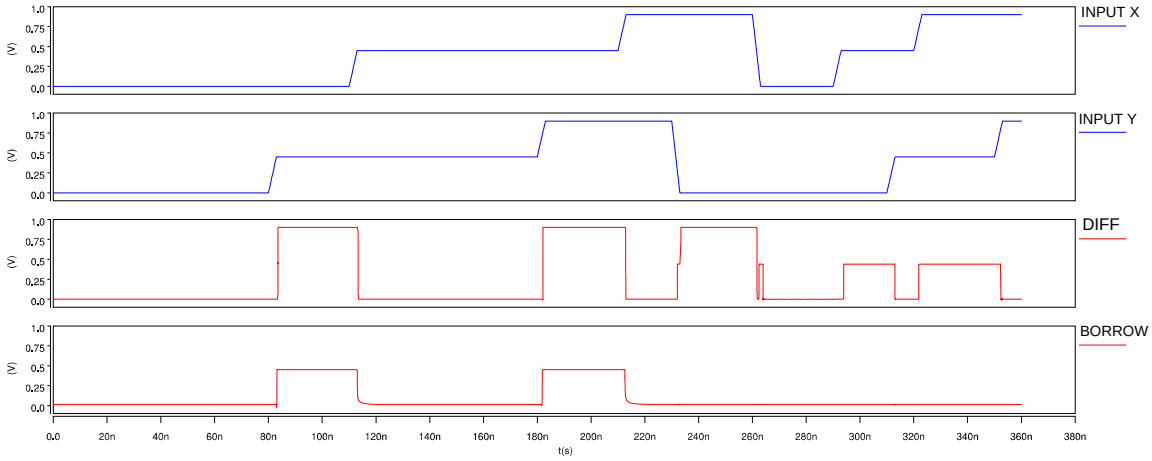


Figure 12. Input and Output waveforms of Ternary Half Subtractor.

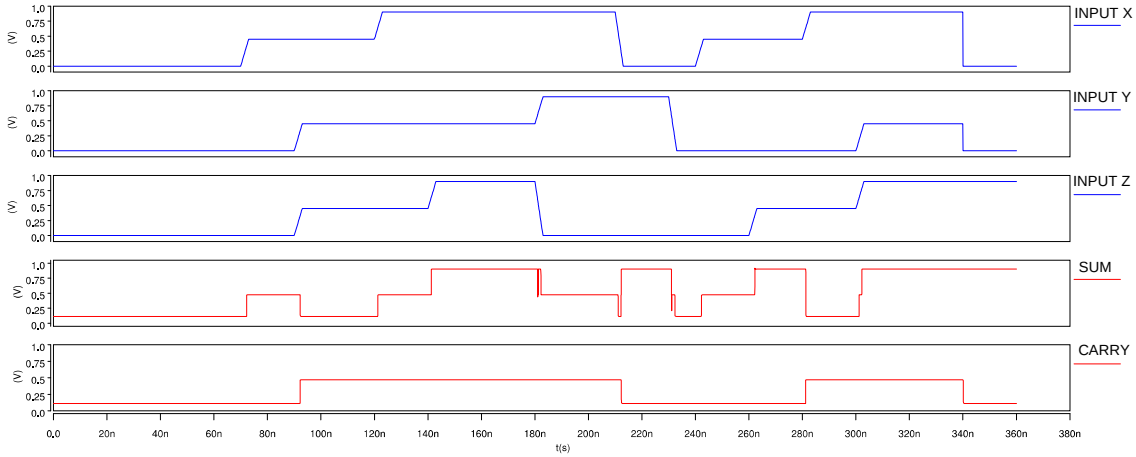


Figure 13. Input and Output waveforms of Ternary Full Adder.

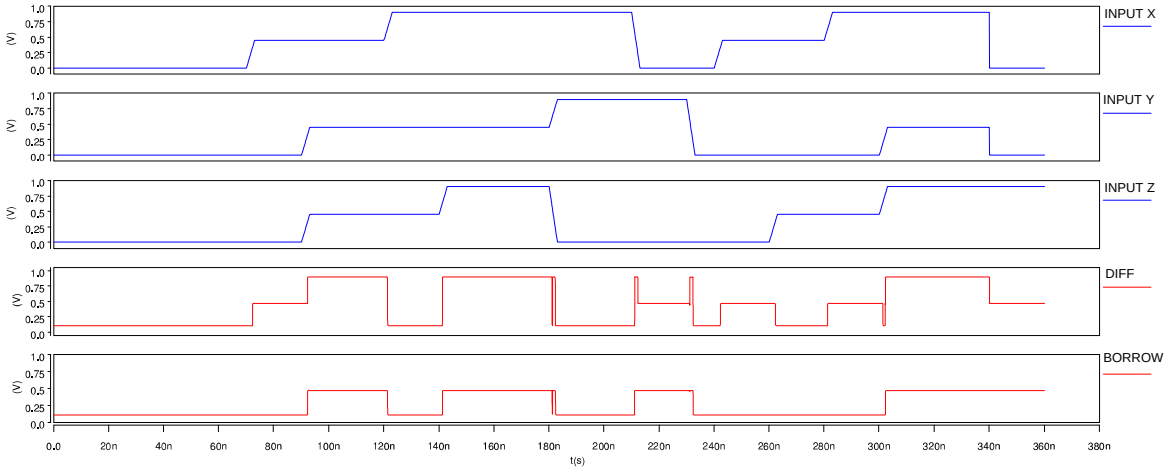


Figure 14. Input and Output waveforms of Ternary Full Subtractor.

4.2. Performance Comparison

The schematic of ternary half adder and half subtractor circuits is composed of two ternary decoders, which are implemented while using CNTFET-RRAM ternary logic gates, nine two-inputs binary NAND, two three-inputs binary NAND, two binary inverters, two proposed two-inputs TNAND, and one proposed level shifter. Table 6 lists the component count (both transistors and RRAM) of the ternary half adder and the ternary half subtractor designs.

Similarly, the schematic of ternary full adder and full subtractor circuits is composed of three ternary decoders, which are implemented while using CNTFET-RRAM ternary logic gates, four two-inputs binary AND, twenty two three-inputs binary AND, seven three-inputs binary OR, one four-inputs binary OR, two proposed three-inputs TOR, three proposed two-inputs TOR, two proposed two-inputs TNAND, and three binary inverters. Table 7 lists the component count (both transistors and RRAM) of the ternary full adder and the ternary full subtractor designs.

The comparison of the transistor count for ternary half adder, ternary half subtractor, ternary full adder, and ternary full subtractor with the existing designs is depicted in Table 8. This comparison of the proposed circuits demonstrates a notable reduction in the transistors count. The reduction in the number of transistors of ternary half adder and half subtractor is 6.67% compared to the ternary half adder and ternary half subtractor in [17], 25% as compared to [28], 38.23% when compared to [32], 67.44% as compared to [33], 6.7% when compared to [42], and 25% as compared to [43].

Similarly, for the case of ternary full adder and ternary full subtractor, the comparison is depicted in Table 7. For the ternary full adder and ternary full subtractor, transistor count reduction of around 13.14% as compared to the ternary full adder and full subtractor in [28], 18.20% when compared to [32], 51.71% as compared to [33], and 15.11% when compared to [43] is observed.

For realizing ternary half adder and ternary half subtractor, CNTFET-RRAM ternary logic gates are used and the design optimization is achieved by utilizing the negation of literals technique, in addition to the use of modified level shifter circuit. However, in the case of ternary full adder and ternary full subtractor circuits, we only use CNTFET-RRAM ternary logic gates and the negation of literals approach. The modified level shifter circuit employed in ternary half adder and ternary half subtractor designs in addition to having lesser transistors requires half the supply voltage ($V_{dd}/2$) as compared of the level shifter encoder circuit used in the previous reported designs, which also helps in reducing the power consumption. Thus, the power consumption of the ternary half adder and ternary half subtractor is significantly lower. The modified level shifter circuit cannot be incorporated in the ternary full adder and ternary subtractor designs, thus they have relatively higher power consumption, but, still, the power consumption values are comparable to the existing designs. However, the ternary full adder and the ternary full subtractor designs have significantly lower transistor count, due to the integration of CNTFET-RRAM technology and the added feature of non-volatility due to the presence of RRAM.

Table 6. Component Count (transistors and RRAM) of the proposed Ternary Half Adder and Half Subtractor circuits.

Design	Device Count	Transistor Count	Sub Total *	No. of RRAM
Proposed TDecoder	2	10	20	2
Binary 2-NAND	9	4	36	-
Binary 3-NAND	2	6	12	-
Binary NOT	2	2	4	-
Proposed 2-TNAND	2	5	10	2
Proposed Level Shifter	1	2	2	-
Total			84 Transistors	4

*** Sub Total= Device Count × Transistor Count.**

Table 7. Component Count (transistors and RRAM) of the proposed Ternary Full Adder and Full Subtractor circuits.

Design	Device Count	Transistor Count	Sub Total *	No. of RRAM
Proposed TDecoder	2	10	20	2
Binary 2-AND	4	6	24	-
Binary 3-AND	22	8	176	-
Binary 3-OR	7	8	56	-
Binary 4-OR	1	10	10	-
Proposed 2-TNAND	2	5	10	2
Proposed 2-TOR	3	8	24	6
Proposed 3-TOR	2	10	20	4
Total			337 Transistors	14

*** Sub Total = Device Count × Transistor Count.**

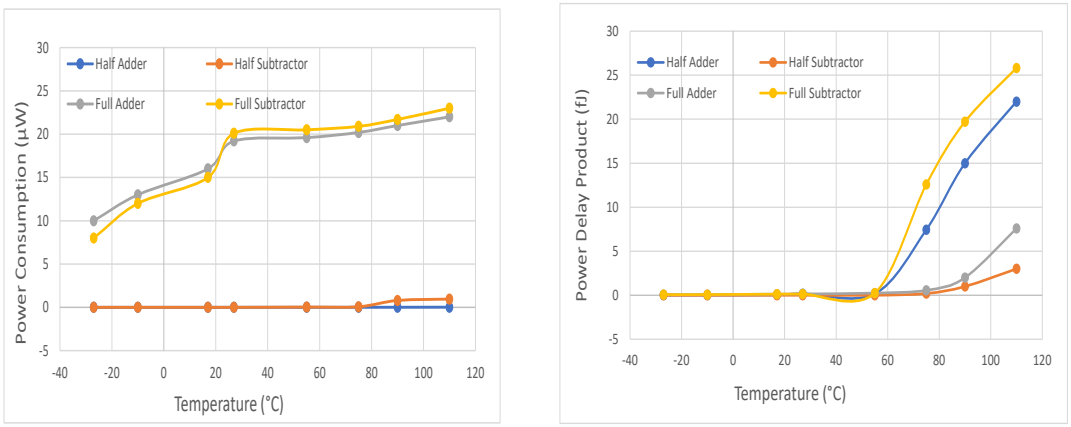
Table 8. Transistor count comparison of Ternary Combinational Logic circuits.

DESIGN	Ternary Half Adder	Ternary Half Subtractor	Ternary Full Adder	Ternary Full Subtractor
Zahoor et.al. [17]	90	90	-	-
Samadhi et.al. [28]	112	112	388	388
Lin et.al. [32]	136	136	412	412
Sridevi et.al. [33]	258	258	698	698
Jaber et.al. [42]	90	90	-	-
Sandhie et.al. [43]	112	112	397	397
Proposed	84	84	337	337

In this study, we also investigate the effect of varying the operating temperature on the circuit performance, as temperature is among the significant factors that negatively degrade the circuit performance. The effect of temperature variation on the performance metrics (power consumption and power delay product (PDP)) of ternary half adder, ternary half subtractor, ternary full adder, ternary full subtractor circuits, respectively, and the same is depicted in Figure 15a,b, respectively. From the observations, we conclude that there is a small variation in the power consumption and PDP over wide temperature ranges, thus having a negligible effect on circuit performance.

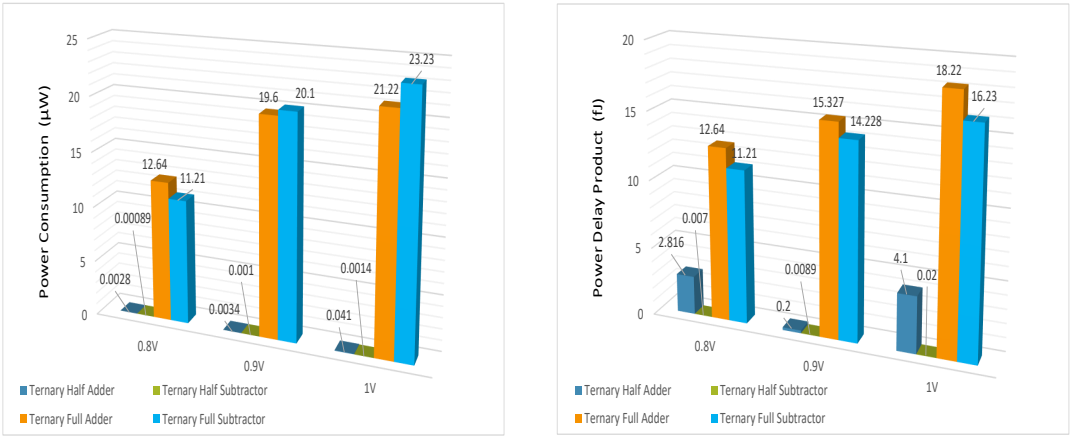
Similarly, we study the performance of the proposed ternary combinational logic circuits, with different supply voltages. Figure 16a,b demonstrates the effect of variation of supply volatge on the power consumption and power delay product of the proposed ternary half adder, ternary half subtractor, ternary full adder, and ternary full subtractor circuits, respectively. The results that were obtained from the simulations, show minimum variation in performance metrics of the proposed ternary designs with varying supply voltage.

Although digital circuits are inherently noise-tolerant, they are only affected by noises with high amplitude and wide width. We take the plot of Noise Immunity Curve (NIC) into account in order to determine the effect of input noise on the ternary half adder circuit. The noise signal depicted in Figure 17a, having pulse width (W_n) and pulse amplitude (V_n), is injected into the inputs of ternary half adder. Figure 17b, depicts the NIC for the CNTFET-RRAM ternary half adder. Each point on the NIC represents a pair of (W_n, V_n), above which the output will have an error. The region above the NIC point is an unsafe zone, whereas the region below is a safe zone against noise pulses. Thus, any circuit with higher NIC demonstrates a more noise tolerant circuit. From the NIC, we conclude that the proposed CNTFET-RRAM ternary half adder circuit demonstrates a good tolerance to the input noise sources.



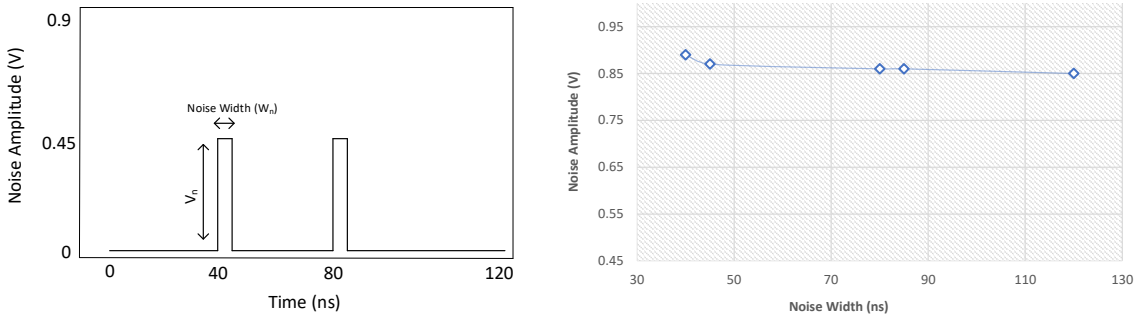
(**a**) (**b**)

Figure 15. Effect of varying operating temperature on (**a**) Power Consumption (**b**) Power Delay Product.



(**a**) (**b**)

Figure 16. Effect of varying operating voltage on (**a**) Power Consumption (**b**) Power Delay Product.



(**a**) (**b**)

Figure 17. Plot of (**a**) Input Noise Signal (**b**) Noise Immunity Curve (NIC).

5. Conclusions

The implementation of computing systems utilizing ternary logic designs has come to the fore in recent years, owing to the significant research that has focussed on emerging technologies. This manuscript utilizes the CNTFET and RRAM for implementing combinational ternary logic circuits. The proposed ternary designs (half adder, half subtractor, full adder, and full subtractor) have been implemented and simulated wile using HSPICE and the results obtained from the simulation confirm the proper functionality of the proposed designs. When compared to the existing designs, the proposed ternary designs are superior in terms of the transistor count, power consumption, and reduced area. Therefore, on the basis of the results that were obtained from the simulations, we deduce that the proposed methodology is an effective solution for reducing the component count, complexity of the hardware, power consumption, and cost of the design. In addition, the proposed designs are analyzed under various operating conditions, with varying supply voltages and different operating temperatures, in order to confirm the robustness of the designs.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

RRAM	Resistive Random Access Memory
CNTFET	Carbon Nanotube Field Efect Transistors
STI	Standard Ternary Inverter
NTI	Negative Ternary Inverter
PTI	Positive Ternary Inverter
NIC	Noise Immunity Curve

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