British Journal of Mathematics & Computer Science
4(9): 1240-1245, 2014

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Comparison between Spartan-3E and Virtex-6 Technologies on FPGA for UART Transmission

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Original Research Article

Received: 24 October 2013
Accepted: 31 January 2014
Published: 27 February 2014

Abstract

This paper presents the hardware implementation of high speed (Universal Asynchronous Receiver/Transmitter) UART using (Field Programmable Gate Array) FPGA. UART is an integrated circuit containing a transmitter (parallel to serial converter) and a receiver (serial to parallel converter) each clocked separately. It transmit 9600 to 34800 bps for transmitting data bit. A high speed UART using 90nm and 40nm technologies has been designed by using FPGA's Spartan 3E and Virtex 6 synthesized on the xilinx ISE 12.4i in VHDL language. By comparing these two technologies on the basis of number of slices, look up tables, GCLK's, slice flip-flops and maximum frequency, it was seen that 40nm technology consumes less area and is 3 times faster than 90nm technology.

Keywords: *UART; FPGA; VHD; XILINX ISE; LUT's; CLBs.*

1 Introduction

An UART is a silicon microchip with programming that controls a computer's interface to its attached serial devices. Specifically, it provides the computer with the RS-232C DTE interface so that it can talk to and exchange data with modems and other serial devices. The UART consists of a transmitter, a baud rate generator and a receiver [1].

The rate at which the data is transmitted is known as Baud rate [2]. UART is mainly used because of its high speed, lesser cost and more fidelity as compared to ASICs. There are two primary forms of serial communication: synchronous and asynchronous [3]. Synchronous serial transmission requires that the sender and receiver share a clock with one another or that the sender provide a strobe or other timing signal so that the receiver knows when to "read" the next bit of the data [4]. In most form of serial synchronous communication, if there is no data available at a given instant to transmit, a fill character must be sent instead so that data is always

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being transmitted [5] Asynchronous transmission allows data to be transmitted without the sender having to send a clock signal to the receiver [6]. Asynchronous serial communication because of less transmission line, high reliability and long transmission distance is usually implemented by UART [7]. VHDL has been used to implement core functions of UART and integrate them into a FPGA chip [8]. As we are using Finite State Machine for transmitter due to which our design has become less complex and the proposed UART becomes more stable, reliable and compact for serial data transmission [9]. Due to which, the consumption of LUT's, flip-flops or in short the area consumption of the chip becomes less. We have also tested our design for the errors which arises during transmission of data to analyze that our output is free from the errors [10].

2 Methodology

VHDL code for UART transmitter is designed. VHDL programs have been implemented and tested on XILINX project Navigator Release 12.4i. Device utilization of higher (40nm) and lower (90nm) technology is taken. Timing summary of both technologies is taken. The performance of modified UART transmitter is evaluated by giving the tight timing constraints which provide better results than corresponding section at lower technology. Fig. 1 shows the flow chart of UART transmitter and explains the functionality of transmitter that how data has been transmitted.

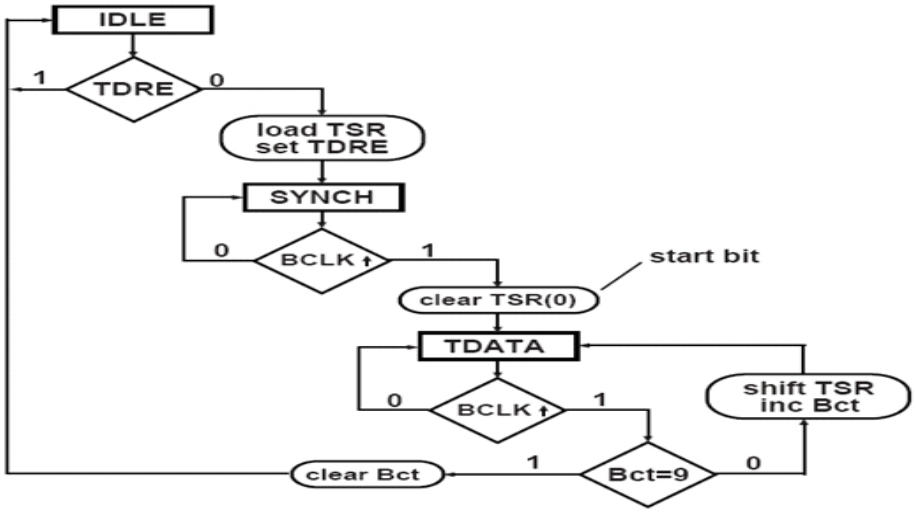

Fig. 1. Flow chart of UART transmitter

3 Results

After implementation of VHDL code, Fig. 2 shows the Block diagram of UART Transmitter. Figs. 3 and 4 show the RTL and Technology Schematic generated by the tool.RTL Schematic shows basic gates (like and, or, nand, nor, not etc), combinational circuits (like mux etc) and sequential circuits (flip-flops). Technology Schematic shows basic blocks i.e. configurable logic blocks (CLBs of FPGA). The CLBs of FPGA consist of look up tables LUT, buffer, mux and flip-flop. CLBs are the programmable logic components of FPGA. A logic block consists of a few

logical cells called slices. CLBs are surrounded by a powerful hierarchy of versatile routing resources. FPGA manufacturers try to provide just enough tracks so that most designs that will fit in terms of LUTs and IOs can be routed. Table 1 shows the comparison of two different technologies i.e. lower technology (90nm-spartan3E) and higher technology (40nm-virtex6) on the basis of number of slices, look up tables, GCLK's, slice flip-flops and maximum frequency. While doing comparison it is found that virtex technology shows great significance as all the parameters are consuming less area and giving results at faster rate.

Table 1. Comparison between Spartan and Virtex technologies

Category	Spartan technology	Virtex technology
Target Device	XC3S100E-5VQ100	XC6VLX75T-3FF484
Technology	90 nm	40 nm
Number of slices	1% (18/960)	0% (24/93120)
Number of slice FF'S	1% (24/1920)	0% (38/46560)
Number of 4 I/P LUT'S	1% (26/1920)	31% (15/47)
Number of bonded IOBs	22% (15/66)	6% (15/240)
Number of GCLKs	4% (1/24)	3% (1/32)
Maximum Frequency	198.098MHZ	735.998MHZ

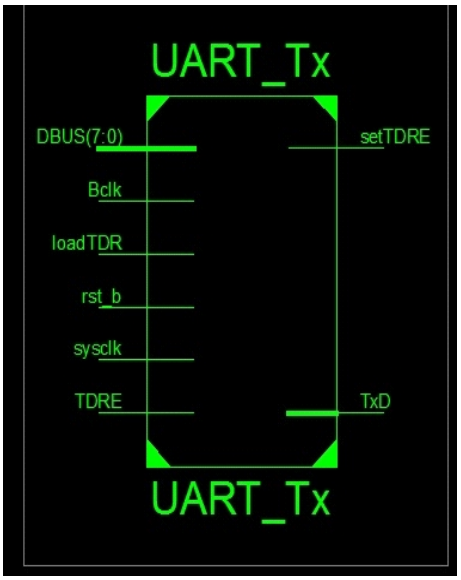

Fig. 2. UART Transmitter implemented in Xilinx ISE

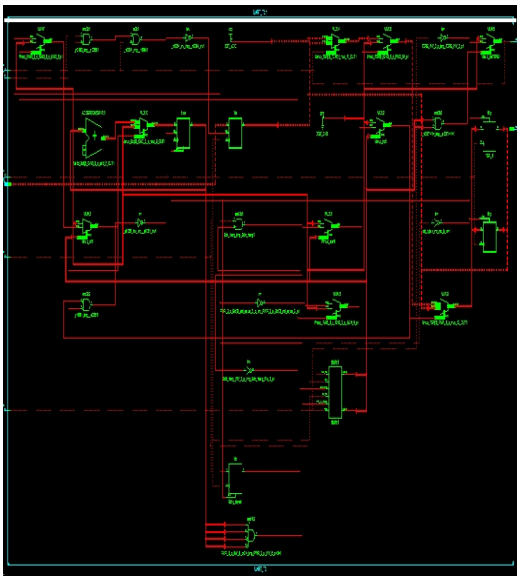

Fig. 3. RTL Schematic of UART Transmitter

The VHDL programs have been implemented and tested on Xilinx Project Navigator Release ISE 12.4i. After implementation of VHDl code of UART Transmitter, RTL and technology schematic is generated by the tool as shown in Fig. 2. The RTL schematic is generated by execution of RTL synthesizer which converts VHDL code into RTL schematic made up of basis gates, combinational circuits and sequential circuits as shown in Figs. 3 and 4 shows the technology schematic as generated by execution of technology synthesizer which converts basic VHDL into

technology schematic. It is made up of basic blocks of FPGA such as LUT, buffer, mux and flip flops.

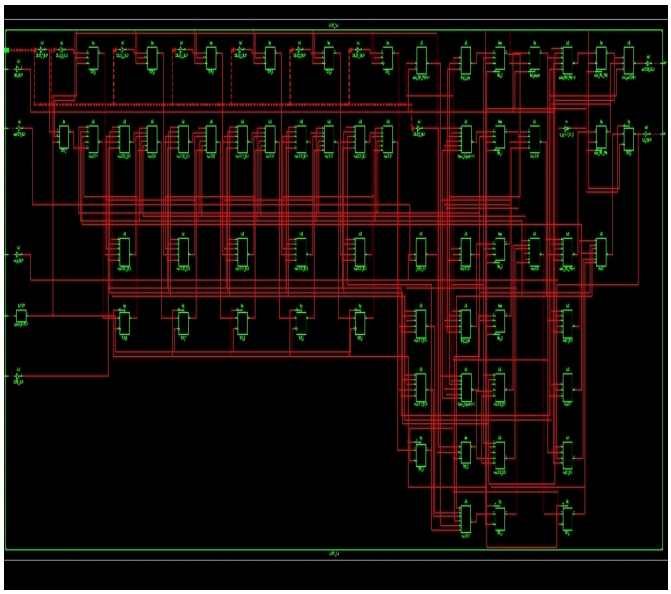

Fig. 4. Technology schematic of UART transmitter

Table 2 shows the timing summary of UART Transmitter implemented on 90nm and 40nm FPGA kit in which time used by 40nm FPGA kit to produce output is 1.421ns as compared to 4.341ns time taken by 90nm FPGA kit at a frequency of 703.532MHz and 230.346MHz respectively.

Table 2. Timing summary

Category	UART Transmitter implementation on 90nm FPGA kit	UART Transmitter implementation on 40nm FPGA kit
Minimum period	4.341ns (Maximum Frequency: 230.346MHz)	1.421ns (Maximum Frequency: 703.532MHz)
Minimum input arrival time before clock	5.086ns	1.220ns
Maximum output required time	5.362ns	1.075ns
Maximum combinational path delay	5.895ns	0.846ns

4 Conclusions

The purposed modified UART transmitter section using higher technology at 40nm work which is 3 times faster than the transmitter section implemented at lower technology 90nm. The performance is evaluated by giving the tight timing constraints which provide better results than

corresponding section at lower technology. The result of present study revealed that by using 40nm technology with improved architecture can enhance the speed of UART by 3 times the 90nm technology. This implementation uses VHDL to get the modules of UART. After studying the comparative analysis it was seen that the results are quiet stable and reliable which provide high bps rate.

5 Future Scopes

The study can be further extended to the following issues:

- The study only includes transmitter section of UART and further work could be done in receiver section.
- The performance of UART can be analyzed for different architecture so as to get optimum results.
- Moreover, the study could be extended as power analysis in terms of transmitter and receiver.

Competing Interests

Authors have declared that no competing interests exist.

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