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HIGH PERFORMANCE WALLACE TREE MULTIPLIER USING IMPROVED ADDER

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Abstract

Multiplier is a crucial block of most of the digital arithmetic applications. With the advancement in the field of VLSI, achieving high speed and low power consumption has become a major concern for the designers. As multiplier block consumes large amount of power and has a major role to play in the speed of the circuit therefore its optimization will improve the performance of the circuit. The process of multiplication is implemented in hardware using shift and add operation, so use of efficient adder circuit will lead to improved multiplier. In this paper, reduced complexity Wallace tree multiplier circuit is proposed that uses efficient and improved adder. The circuits are designed using 90nm technology and simulated in Cadence Virtuoso. The proposed Wallace tree structure offers a decrement of approximately 70% in dissipation of power, approximately 86% in power delay product and 60% in area. The proposed multiplier is suitable to use in applications such as DSP structures, ALU's and several low power and high speed arithmetic applications.

Keywords:

Wallace Tree, Full Adder, Pass Transistor Logic, Power Dissipation, Delay

1. INTRODUCTION

With the increase in integration scale, more and more advanced and compact signal processing systems are needed to be actualized on VLSI chip. These processing applications consume a hefty amount of power and require good computation capacity. With performance and area, power dissipation has also become a concerning factor for design of integrated circuits. There are two main factors that led to this budding of low power systems. Firstly, increased integration has led to increase in processing capacity due to which large flow of currents takes place leading to heating up of the chip. Secondly in portable electronic devices the battery life is limited and hence prolonged operation of these portable devices can be obtained by achieving low power design.

It is known that in most of the signal processing algorithms, multiplication have a fundamental role to play. The system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. All the multipliers use full adders and hence can be optimized using the modified full adders.

In this paper, authors have proposed a compact Wallace tree multiplier structure to meet the present day needs of low power and high speed applications. The paper is dived as follows. The proposed multiplier uses improved adder designed using pass transistor logic in 90nm technology. The proposed adder offers lesser delay and area than the conventional techniques discussed in literature.

The paper is organized as follows: Section 2 discuss the conventional approaches. Section 3 presents the proposed Wallace Tree structures. The results and discussion are compiled in section 4. Section 5 concludes the paper.

2. WALLACE TREE MULTIPLIER

The important design consideration for any chip designer are power consumption, delay and area. Speed of the circuit changes with the speed/delay of the multiplier therefore a lot of research has been done to increase the speed of multiplier so that delay of the overall circuit can be reduced. Wallace Tree is a high speed and area efficient multiplier and is therefore of great importance in high speed applications [1].

It implements easy and efficient hardware methodology that multiplies integers using the column compression technique. Wallace tree offers fast speed because instead of linear dependency as in array multiplier, the total delay is proportional to the logarithm of word length of the operand of multiplier. The operation of Wallace Tree Multiplier involves three steps: formation of partial products, grouping of these formed partial products and addition using adders.

To improve the performance of Wallace Tree lot of research has been done [2-8]. In [2], author has proposed to use parallel prefix adders instead of conventional half and full adders in Wallace multiplier, leading to reduction in delay but the area and power dissipation constraints are not looked into. In [3], to reduce area and latency booth encoding with compressor approach is used.

Further in [4], XOR-XNOR based 3:2, 4:2 and 5:2 compressors are used in place of half and full adders in second stage of Wallace algorithm, leading to increase in speed. Though [3] and [4] has led to improvement in the speed of the multiplier but the area is not reduced considerably and also the use of 4:2 and 5:2 compressors increases the complexity resulting in complex routing. Improvement is also done by estimating power using probabilistic gate level power estimator in each stage [5] or by rearranging the partial products in such a way so that switching activity is reduced.

This offers a significant power reduction but area and speed remains unaltered. Besides this the improvement depends on the transition activity of the inputs. In [6], a full adder using 4:1 multiplexer is used in reduction phase leading to power reduction. In [7], full adder using 2:1 multiplexer is used also reducing power. These techniques of implementing full adder has led to power reduction but the critical path delay is more than that of [8]. From all the previous studied literature [8] offers the best performance on ground of area, power and speed. The Fig.1 shows the schematic of the adder used in [8].

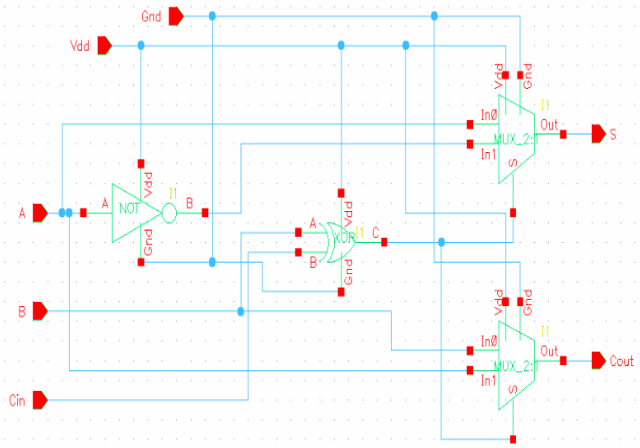

Fig.1. Conventional Full Adder [8]

3. PROPOSED WORK

As discussed in the previous section of the paper Wallace Tree multiplier offers best speed compared to other multiplier circuits and hence various techniques to improve its structure have been proposed as discussed in [2-8]. In this paper a modified wallace tree structure has been proposed that offers better performance compared to existing approaches. The proposed structure is designed using reduced complexity algorithm [9-10] and modified adder subcircuit to process the intermediate addition of bits. The Fig.2 shows the proposed adder, designed using Pass Transistor Logic based 2:1 multiplexers. The Fig.3 displays the 2:1 pass transistor based mux. The use of pass transistor logic has led to considerable decrease in number of transistors and hence the area. Besides this it has best advantage of least static leakage. Due to very few Vdd to ground connections during switching the short circuit power is also least. The modified expressions for the sum and carry of the full adder circuit are given as following Eq.(1) and Eq.(2):

$$\begin{aligned} SUM &= A \,\text{XOR}\, B \,\text{XOR}\, C \\ &= (A \,\text{XOR}\, B) \,\text{XOR}\, C \\ &= \left((AB)' + AB\right)C + \left(A'B + AB'\right)\text{C} \\ &= (AB)'C + ABC + A'BC' + A(BC)' \\ &= A\left(B'C + BC'\right) + A'\left(B'C + BC'\right) \\ &= \left((B \,\text{XOR}\, C)'\right)A + (B \,\text{XOR}\, C)A' \end{aligned} \quad (1)$$

$$\begin{aligned} CARRY &= AB + BC + CA \\ &= C(B + A) + AB \\ &= C(B + A)\left(B + B'\right) + AB \\ &= B(C + A)\left(C + C'\right) + ACB \\ &= BC + ABC' + ACB' \\ &= B\left((B\,XOR\,C)'\right) + A(B\,XOR\,C) \end{aligned} \quad (2)$$

Working of the circuit can be explained as follows and is verified from the truth table as shown in Table.1. If $B = C = 0/1$ then *Sum* = *A* and *Carry* = *B*. If *B* != *C* then *Sum* = *A*! and *Carry* = *C*.

In our proposed Wallace Tree Structure this modified adder is used alongwith the reduced complexity algorithm for wallace tree multiplier [9-10]. Unlike conventional wallace multiplier in which both full adders and half adders are used to process three and two bits respectively, it uses only full adders unless the number of stages remain equal to that of conventional wallace algorithm. The performance of multiplier is not affected by eliminating half adders as they don't compress the number of partial bits, two bits added gives two bits in output (Sum and Carry).

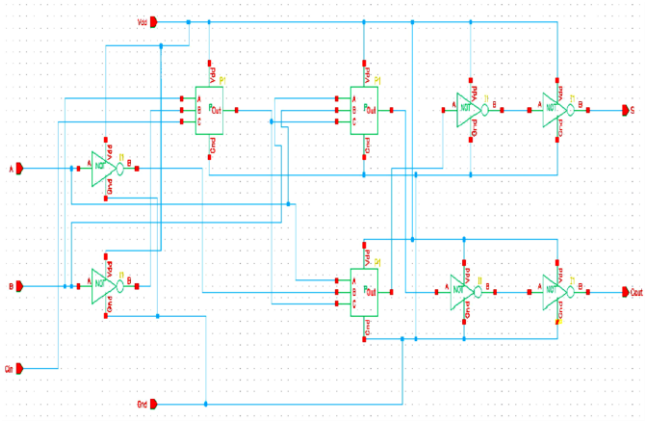

Fig.2. Proposed Adder

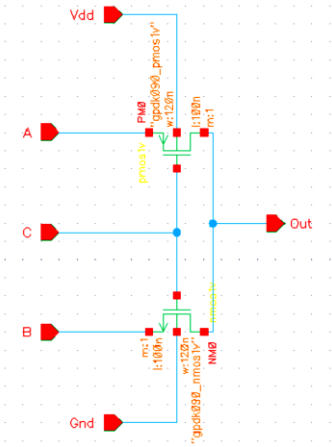

Fig.3. Pass Transistor Logic Based 2:1 Multiplexer

Table.1. Truth Table of Proposed Adder

A	B	C	Sum	Carry
0	0	0	0(A)	0(B)
0	0	1	1(~A)	0(A)
0	1	0	1(~A)	0(A)
0	1	1	0(A)	1(B)
1	0	0	1(A)	0(B)
1	0	1	0(~A)	1(A)
1	1	0	0(~A)	1(A)
1	1	1	1(A)	1(B)

The Fig.4 shows 4×4 bit multiplication using reduced complexity algorithm. It can be seen that only S3 and C2 are

processed as two bits so that number stages does not exceed the conventional approach. The intermediate addition are performed by using the proposed adder. The proposed wallace tree multiplier structure is show in Fig.5.

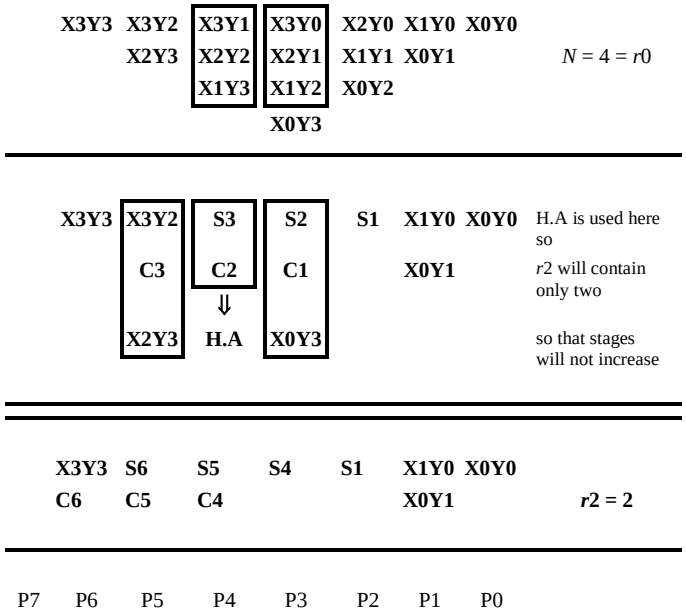

Fig.4. 4×4 bit Multiplication using Reduced complexity Wallace Algorithm

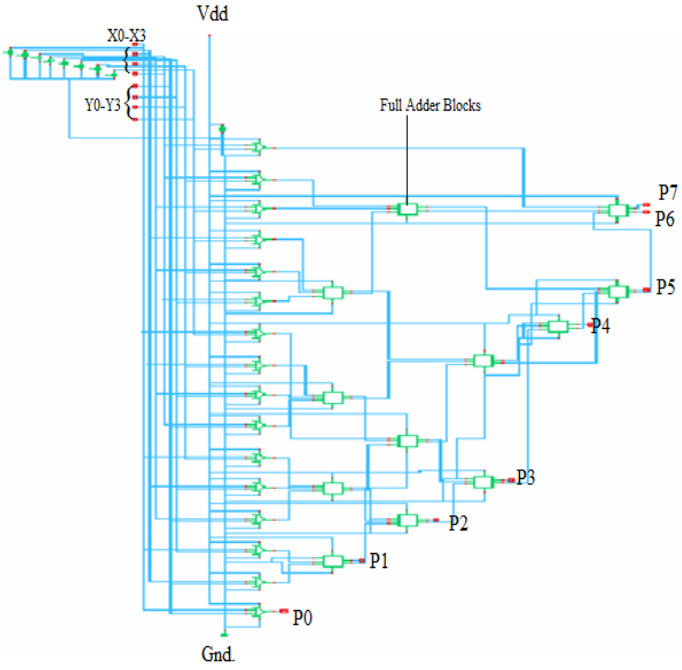

Fig.5. Proposed 4×4 bit Wallace Tree Multiplier

4. RESULTS

Simulations of all the circuits were performed in Cadence Virtuoso using 90nm technology. The proposed adder has been compared with the conventional version of [8] in Table.2.

The Fig.6 and Fig.7 shows the result for the conventional and proposed adder. From the output waveforms it is observed that circuit perform the correct functionality. For the sake of comparison from the conventional circuits of [8], same inputs were given to both the full adders.

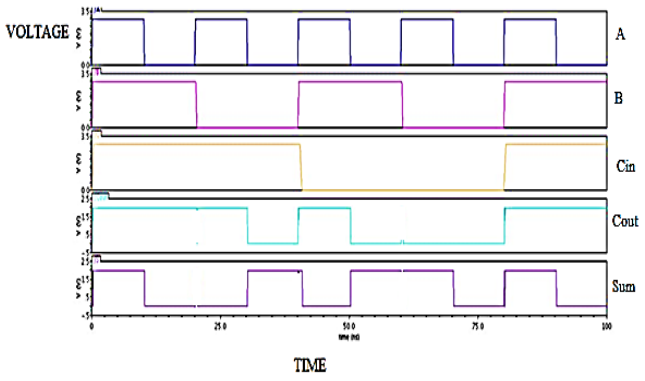

Fig.6. Output Waveform of Proposed Adder

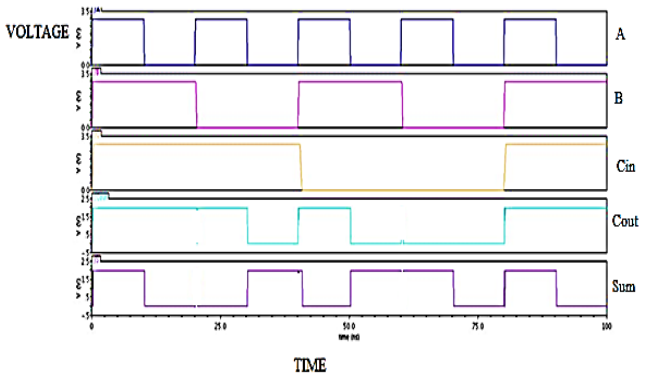

Fig.7. Output Waveform of Conventional Adder

Table.2. Comparative Result of Adders

Adder Circuit	Existing Adder	Proposed Adder
No. of Transistor	56	18
Delay (ps)	60.58	48.48
Logic Used	CMOS XOR gate + Mux	Pass Transistor Logic

From Table.2, it is observed that the area i.e number of transistors and the delay of the proposed adder has been reduced considerably from the conventional adder.

Simulated results of the proposed wallace tree structure and shown in Fig.7. The Table.3 summarizes the obtained results of the wallace tree structures. It can be seen that number of transistors are considerably reduced in the proposed wallace tree structure.

This reduction has led to reduction in the power dissipation in wallace structures i.e. the power that is dissipated due switching activity of the pass transistor logic is less compared to the power that is dissipated by the extra number of transistor in the conventional wallace structure. Also the power delay product is less compared to the conventional.

The Fig.10, Fig.11 and Fig.12 shows the layout of the proposed adder block, pass transistor 2:1 multiplexers and the not

gate respectively. The layout of proposed adder has been made 48.5 × 30.9µm boundary using design rules for 90nm technology and finally GDSII file was generated.

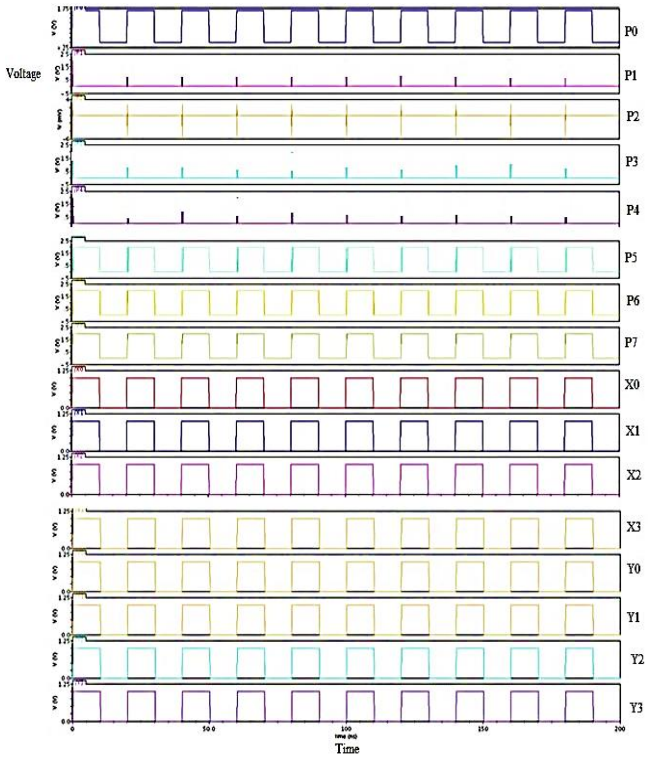

Fig.8. Output Waveform of Proposed RCWTM

The above waveforms of Fig.8 can be explained as follows using the algorithm of Fig.4. Here, X = 1111 AND Y = 1111. Therefore, the after multiplication we get P = 11110001. The Fig.9 shows the algorithmic procedure.

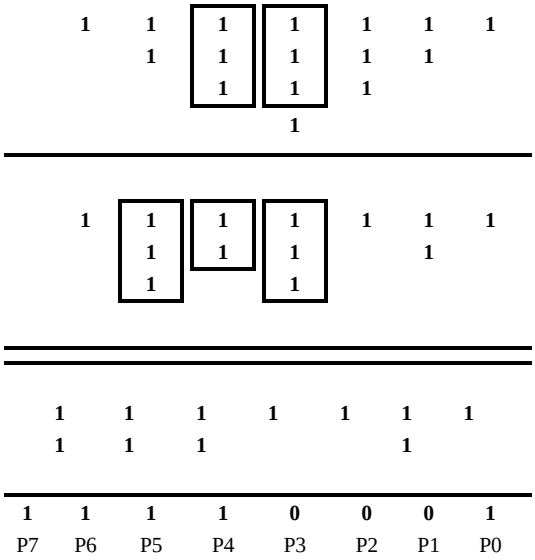

Fig.9. Verification Of Result Of Proposed Multiplier

Table.3. Comparative Study of Wallace Tree Structures

Multiplier Circuit	Exixsting Wallace Tree [9]	Proposed wallace Tree	Percentage improvement
Number of Transistor	768	312	59.3%
Power Dissipation (mW)	2.283	.694	69.6%
Power Delay Product	473.72	65.57	86.1%

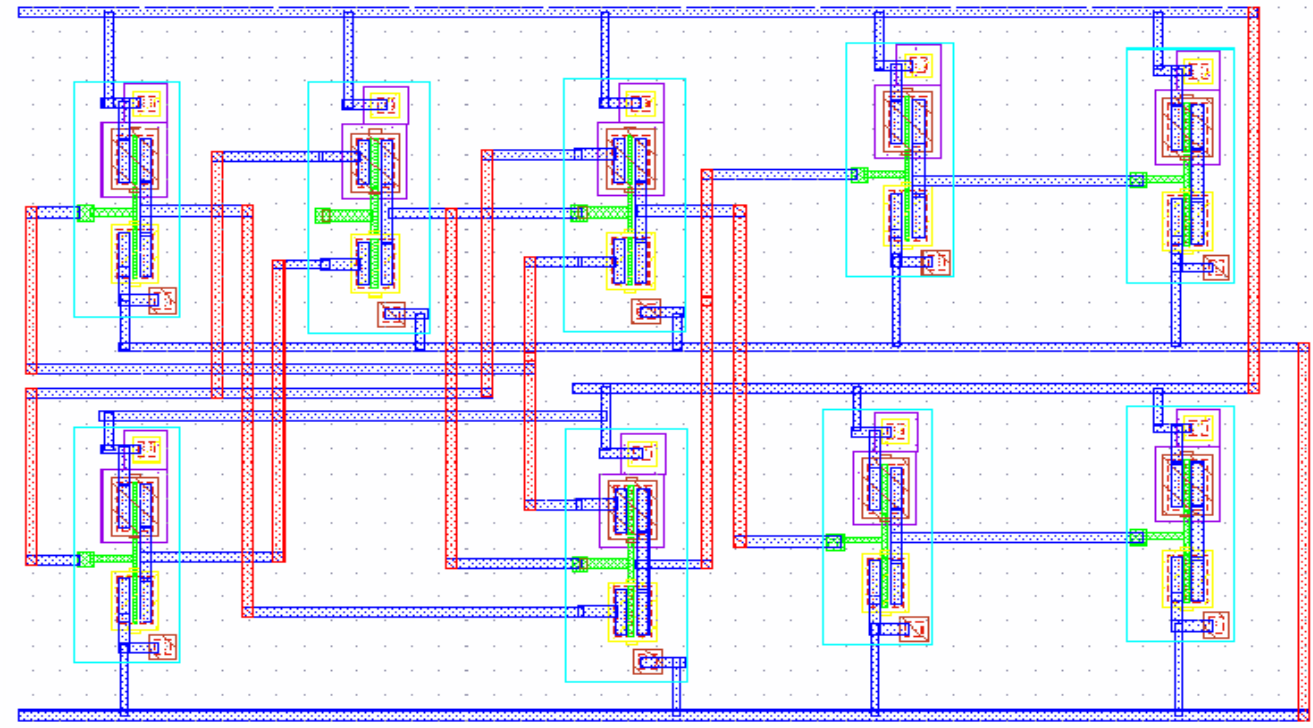

Fig.10. Layout of proposed Adder

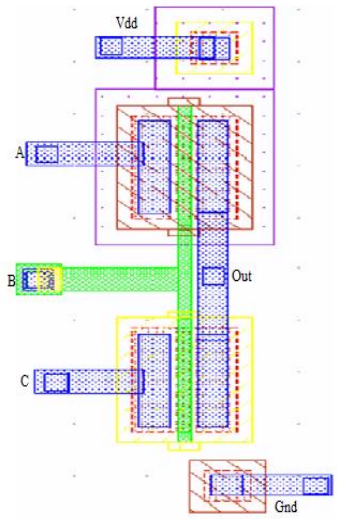

Fig.11. Layout of P.T.L based 2:1 Mux

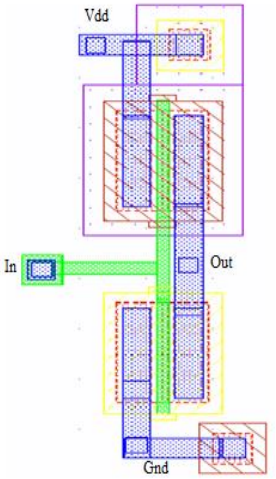

Fig.12. Layout of NOT gate

5. CONCLUSION

In this paper Wallace tree multiplier has been investigated and then modified Wallace tree multiplier circuits were proposed and simulated using 90nm technology in Cadence Virtuoso. Initially we simulated the existing adder and Wallace multiplier proposed in [8]. Then a new improved adder is proposed that uses PTL based 2:1 multiplexer. The number of transistors used is comparatively less than that of existing adder and hence the area is minimized and also delay offered is less.

The proposed Wallace Structure offers an improvement of 59.3% in reduction of power, 86.1% of reduction in power delay product and 60.6% reduction in the number of transistors used i.e. area. The power dissipation, area and power delay product of the proposed Wallace multiplier has been minimized by a considerable magnitude. With the increase in demand of greater speed with less battery usage and minimum area, our proposed structures will prove beneficial in all the applications that perform mathematical operations using multipliers. Some of the applications in which it can be widely used are ALU's and DSP structures.

REFERENCES

[1] C.S. Wallace, "A Suggestion for A Fast Multiplier", *IEEE Transaction on Electronic Computers*, Vol. 13, No. 1, pp. 14-17, 1964.

[2] S. Rajaram and K. Vanithamani, "Improvement of Wallace Multipliers using Parallel Prefix Adders", *Proceedings of IEEE International Conference on Signal Processing, Communication, Computing and Networking Technologies*, pp. 781-784, 2011

[3] M.J. Rao and S. Dubey, "A High Speed and Area Efficient Booth Recoded Wallace Tree Multiplier for Fast Arithmetic Circuits", *Proceedings of Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*, pp. 220-223, 2012.

[4] S. Karthick, S. Karthika and S. Valannathy, "Design and Analysis of Low Power Compressors", *International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering*, Vol. 1, No. 6, pp. 487-493, 2012.

[5] Saeeid Tahmasbi Oskuii, Per Gunnar Kjeldsberg and Oscar Gustafsson, "Power Optimized Partial Product Reduction Interconnect Ordering in Parallel Multipliers", *Proceedings of Nordic Circuits and Systems Conference*, pp. 1-6, 2007.

[6] S. Murugeswari and S.K. Mohideen, "Design of Area Efficient and Low Power Multipliers using Multiplexer based Full Adder", *Proceedings of 2nd International Conference on Current Trends in Engineering and Technology*, pp. 388-392, 2014.

[7] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha and Jin-Gyun Chung, "A Novel Multiplexer-based Low-Power Full Adder", *IEEE Transactions on Circuits and Systems*, Vol. 51, No. 7, pp. 345-348, 2004.

[8] Kokila Bharti Jaiswal, Nitish Kumar, Pavithra Seshadri and G. Laxminarayan, "Low Power Wallace Tree Multiplier using Modified Full Adder", *Proceedings of 3rd International Conference on Signal Processing, Communication and Networking*, pp. 1-4, 2015.

[9] R.S. Waters and E.E. Swartzlander, "A Reduced Complexity Wallace Multiplier Reduction", *IEEE Transactions on Computers*, Vol. 59, No. 8, pp. 1134-1137, 2010.

[10] Sandeep Kakde, Shahebaj Khan, Pravin Dakhole and Shailendra Badwaik, "Design of Area and Power Aware Reduced Complexity Wallace Tree Multiplier", *Proceedings of International Conference on Pervasive Computing*, pp. 1-6, 2015.