


Article

Equivalent Circuit Modeling of a Dual-Gate Graphene FET

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Abstract: This paper presents a simple and comprehensive model of a dual-gate graphene field effect transistor (FET). The quantum capacitance and surface potential dependence on the top-gate-to-source voltage were studied for monolayer and bilayer graphene channel by using equivalent circuit modeling. Additionally, the closed-form analytical equations for the drain current and drain-to-source voltage dependence on the drain current were investigated. The distribution of drain current with voltages in three regions (triode, unipolar saturation, and ambipolar) was plotted. The modeling results exhibited better output characteristics, transfer function, and transconductance behavior for GFET compared to FETs. The transconductance estimation as a function of gate voltage for different drain-to-source voltages depicted a proportional relationship; however, with the increase of gate voltage this value tended to decline. In the case of transit frequency response, a decrease in channel length resulted in an increase in transit frequency. The threshold voltage dependence on back-gate-source voltage for different dielectrics demonstrated an inverse relationship between the two. The analytical expressions and their implementation through graphical representation for a bilayer graphene channel will be extended to a multilayer channel in the future to improve the device performance.

Keywords: graphene field effect transistor; ambipolar conduction; threshold voltage dependence; transconductance; quantum capacitance



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1. Introduction

In the last 50 years, the silicon-based semiconductor industry has been operating successfully. Now in the 21st century, this industry has rapidly developed according to Moore's Law. Hopefully, it will encounter both scientific and technical limits soon. This requires the industry to explore new materials and technologies. The discovery of carbon nanotubes in 1991 by Iijima [1] stimulated more interest to work on graphene. Finally, in 2004, Geim and Novoselov at Manchester University isolated single-layer graphene successfully by an easy mechanical exfoliation method just using a scotch tape [2]. Semiconductor devices made of silicon and III-V materials are serving the purpose of high speed and high integration density, but their application in flexible, bendable, and transparent electronics is not prominent. In the field of transistors, especially for FET (field effect transistor) and MOSFET (metal-oxide semiconductor field effect transistor) technology, graphene is a promising candidate because it shows zero effective mass inside a material. The practical consequence of this fact is the high charge carrier mobility [3]. Graphene with numerous numbers of large sheets is inherently two dimensional (2D). It shows zero bandgap. If we pattern it to ribbons, a nanoscale bandgap opens due to the lateral quantum confinement. The bandgap is inversely proportional to the ribbon width, which becomes a lithographically designable parameter [4]. The high current-carrying capacity [5], the 2D or 1D (one dimensional) atomic structure, and the compatibility with planar technology make graphene an attractive alternative to silicon CMOS (complementary metal-oxide semiconductor). Moreover, graphene-based transistors can bring more benefits to tradi-

tional silicon-made CMOS devices. The benefits include photonic modulator and fast radio frequency switching property [6]. GFET (graphene field effect transistor) may be of single-layer, large area having no bandgap or it may contain bandgap using bilayer or doped. Generally, monolayer, undoped, large-area graphene contains zero bandgap and devices made from this kind of graphene are not suitable for logic operation. Rather, it is suitable for RF (radio frequency) application where complete switching off is not mandatory. Recently, RF graphene MOSFETs with large-area channels showing cutoff frequencies in the gigahertz range were studied [7–9] and 100 GHz cutoff frequency was reported for a 240 nm gate transistor [10]. GFET is potentially useful for frequency multiplication, mixing, amplification, and phase shifting. Memory chips and microprocessors based on silicon with a dimension of 20 nm can serve the purpose of storing huge and different data, but further scaling below 20 nm is still a challenge. Material like graphene with three-dimensional structure can play a great role in development of semiconductor technology [11–13]. Therefore, preferably, it can be used as MOSFET (metal oxide field effect transistor) channel rather than silicon [14]. For higher drift velocity, graphene is superior to silicon, in spite of having higher gate length [15,16]. Overall, graphene is better than silicon in few respects; however, it does not mean that graphene can replace silicon totally. Still there are some limitations in case of graphene, like its lower cutoff frequency and zero bandgap property. We have yet to explore defects, impurities, and contact resistance in the channel of graphene [17–19]. As graphene is considered to be a potential candidate for electronics logic and RF applications, research is going on regarding upgrade of design and fabrication of its FETs. However, the progress is at the initial stage. In order to achieve high performance of GFETs, understanding of detailed device modeling and performance evaluations is necessary. There have been few works, mostly on behavior of GFETs, but they are not sufficient for a clear understanding of device physics and modeling. Thus, we are strongly motivated to work on device physics and modeling of a graphene-based MOSFET using an analytical approach. Then, we implemented a combination of the device modeling and simulation in MATLAB software.

This model is a combination of fundamental theories for single-layer and bilayer graphene FET. In previous literature [20,21], properties for single- and bilayer graphene FET were represented individually. In [22], a small signal model was used to show the GFET equivalent circuit without considering the effect of surface potential and number of layers. Some old works reported fabrication procedure of a few layers and multilayer graphene FET [23,24]. However, this work shows physical configuration and output behavior for both single and bilayer together. Mathematical theories for single- and double-layer graphene FET are mentioned in a single frame. This will make it easy to work with multilayer channel GFET in the future. Multiple layers will help in enhancing current and thermal conductivity in graphene channel [25]. Moreover, this model illustrates a simple demonstration of the Boltzmann equation and some basic transistor derivations in case of output current of bilayer GFET. This is a convenient way to understand the behavior of current and voltages in three different regions of GFET. Top gate- and back gate-dependent surface potential for two layers was compared with a standard model in the bilayer section. Finally, all properties of bilayer GFET were shown through simulation. Overall, based on this concept, an effective single-, bilayer, or multilayer GFET can be designed in the future.

In Section 2, the physical layout of GFET is shown. In Section 3, final simulation of the mathematical modeling is presented with appropriate results and discussion. Capacitance and surface potential dependence, drain current characteristics, transconductance, and transit frequency behavior with different terminal voltages were evaluated in this context. In the last part, the discussion, limitations and future directions are given.

2. Materials and Methods

Figure 1a shows the physical structure of graphene FET in a three-dimensional pattern. Additionally, electrical equivalent circuit of GEFET is shown in Figure 1b. Firstly, the analytical expression for top gate capacitance (C_{top}), back gate capacitance (C_{back}),

and threshold voltage (V_0) is shown for single-layer graphene channel. Next, electronic transport characteristics for hole and electron conduction was analyzed. Relationship between drain current (I_{ds}) and drain-to-source voltage (V_{ds}) was determined. Dependence of drain current (I_{ds}) on gate voltages (V_{gs}) was encountered. Characteristics of channel transconductance (g_m) and transit frequency (f_T) were mentioned. Finally, bilayer validation for different dielectrics was plotted by the relationship between threshold voltage and back-gate-to-source voltage.

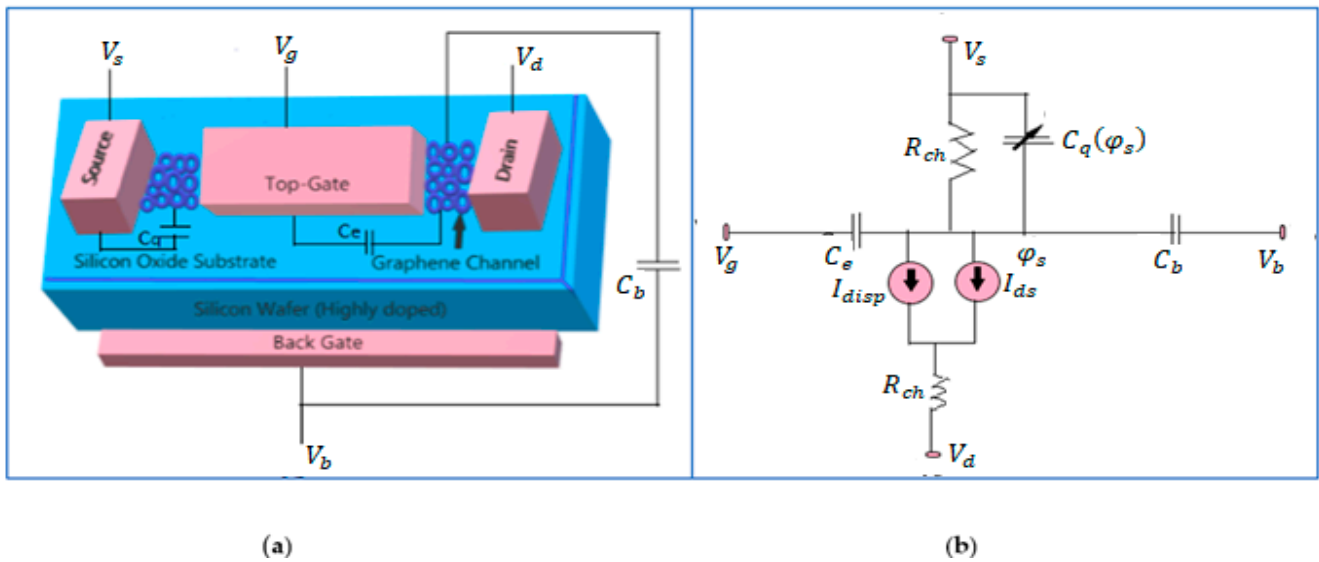


Figure 1. Configuration of a dual-gate graphene field effect transistor. (a) The 3D structure of the transistor. (b) Electrical equivalent circuit.

2.1. Calculation of Threshold Voltage and Surface Potential for Single-Layer Graphene FET

The Dirac point is the crossing point of the linear energy dispersion. Because of two sublattices of graphene, there exist two symmetric Dirac points, $-K$ and $+K$. These are the transitions between the valence band and conduction band. Quantum capacitance can be defined as the variation of electrical charge q with respect to the variation of potential. Variable quantum capacitance in relation to surface potential can be written as [26], where φ_s is the potential change between the graphene channel and the source voltage, V_s ; q is the electrical charge, V_F is the Fermi velocity [27], and \hbar is the reduced Planck's constant. Quantum capacitance depends upon the charge density, and for minimum carrier density n_0 the formula is [20]

$$C_{qmin} = \frac{q^2 \sqrt{n_0}}{\sqrt{\pi \hbar v_F}} \tag{1}$$

We considered capacitance between the top gate and the graphene channel as C_e and C_b is the capacitance between the back gate and the channel. The top gate capacitance due to the effect of top gate potential V_g can be written as

$$C_{top}(\varphi_s) = \frac{C_e C_q(\varphi_s)}{C_e} + C_q(\varphi_s), \tag{2}$$

and the back gate capacitance due to the back gate potential V_b can be expressed as

$$C_{back}(\varphi_s) = \frac{C_b C_q(\varphi_s)}{C_b} + C_q(\varphi_s). \tag{3}$$

Applying capacitive voltage divider formula surface potential can be written as [20]

$$\varphi_s = \frac{C_g(V_{gs} - V_{gs}^0) + C_b(V_{bs} - V_{bs}^0)}{C_g + C_b + C_{qmin} + \frac{1}{2}C_{qvar}(\varphi_s)}. \quad (4)$$

For top-gate-to-source voltage at Dirac point V_{gs}^0 and back-gate-to-source voltage at Dirac point V_{bs}^0 , the threshold voltage is

$$V_o = V_{gs}^0 + \left(\frac{C_{back}(\varphi_s)}{C_{top}(\varphi_s)} \right) (V_{bs}^0 - V_{bs}). \quad (5)$$

Hence, considering Equation (4), quantum capacitance can be stated as

$$C_q = \frac{dq_{net}}{dE_F}. \quad (6)$$

This equation is related to Fermi level E_F . Here, Fermi level can be written as $E_F = q\varphi_s$. $E_F > 0$ and $E_F < 0$ represent electron conduction and hole conduction channel, respectively.

2.2. Surface Potential Calculation for Bilayer Graphene FET

Compared to single-layer structure in bilayer GFET, there is an interlayer capacitance C_0 between two quantum capacitances, as shown in Figure 2a,b.

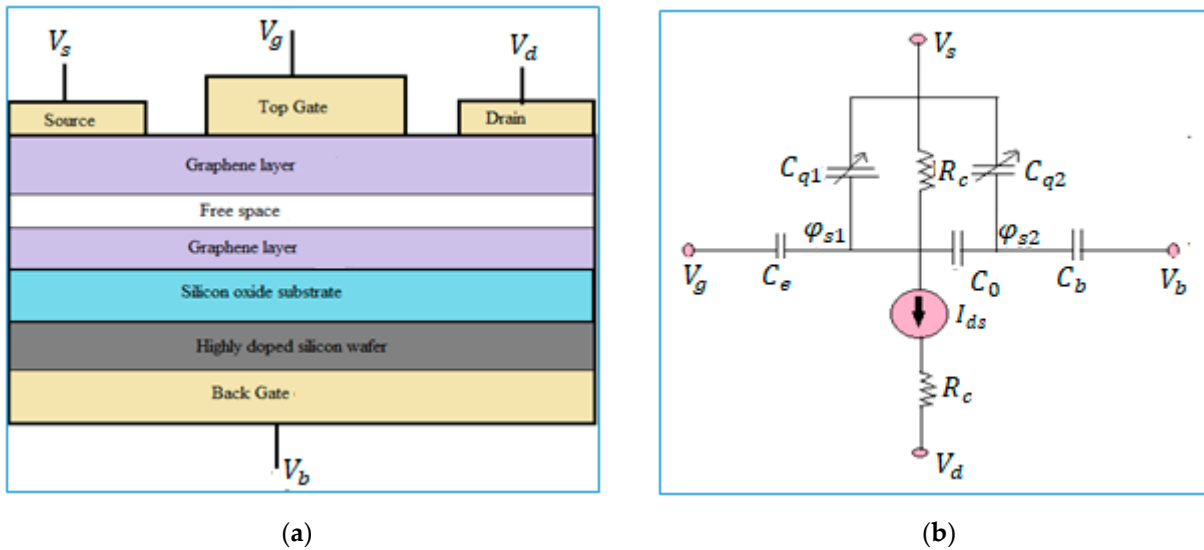


Figure 2. Schematic demonstration of bilayer graphene field effect transistor. (a) Bilayer transistor layout, (b) equivalent model.

According to the equivalent capacitance model of bilayer graphene FET from Figure 1b, surface potential for the first and second layer is [21]

$$\varphi_{s1} = \frac{1}{C_0} [-C_b(V_{bs} - V_{bs}^0) + \varphi_{s2}(C_e + C_0) + \varphi_{s2} \sqrt{\left(\frac{C_q(\varphi_{s2})}{2} \right)^2 + C_{qmin}^2}]. \quad (7)$$

$$\varphi_{s2} = \frac{1}{C_0} [-C_e(V_{gs} - V_{gs}^0) + \varphi_{s1}(C_e + C_0) + \varphi_{s1} \sqrt{\left(\frac{C_q(\varphi_{s1})}{2} \right)^2 + C_{qmin}^2}]. \quad (8)$$

Surface potential of the first layer indicates the position of Fermi level according to its output. Positive value and negative value imply Fermi level is in the conduction band and

valence band, respectively. It locates in the charge neutrality point when output is zero. When surface potential is zero, gate-to-source voltage V_{gs} can be considered as threshold voltage V_{th} and it can be written as $V_{th} = V_{gs}^0 - \varphi_s 2 \frac{C_0}{C_c}$. This theory exhibits similarity with the Fermi level shift in the suspended part from Laitinen equation [28].

2.3. Relationship between Drain Current and Voltages

Figure 3a shows the I-V curve of graphene film. The characteristics can be explained by segmenting it into three sections: the triode region, unipolar saturation region, and ambipolar saturation region. Charge carriers in the first two areas are unipolar (electrons or holes). The curve got squeezed at the drain terminal in the unipolar saturation region. Ambipolar section demonstrates both of the charge carriers (electrons and holes).

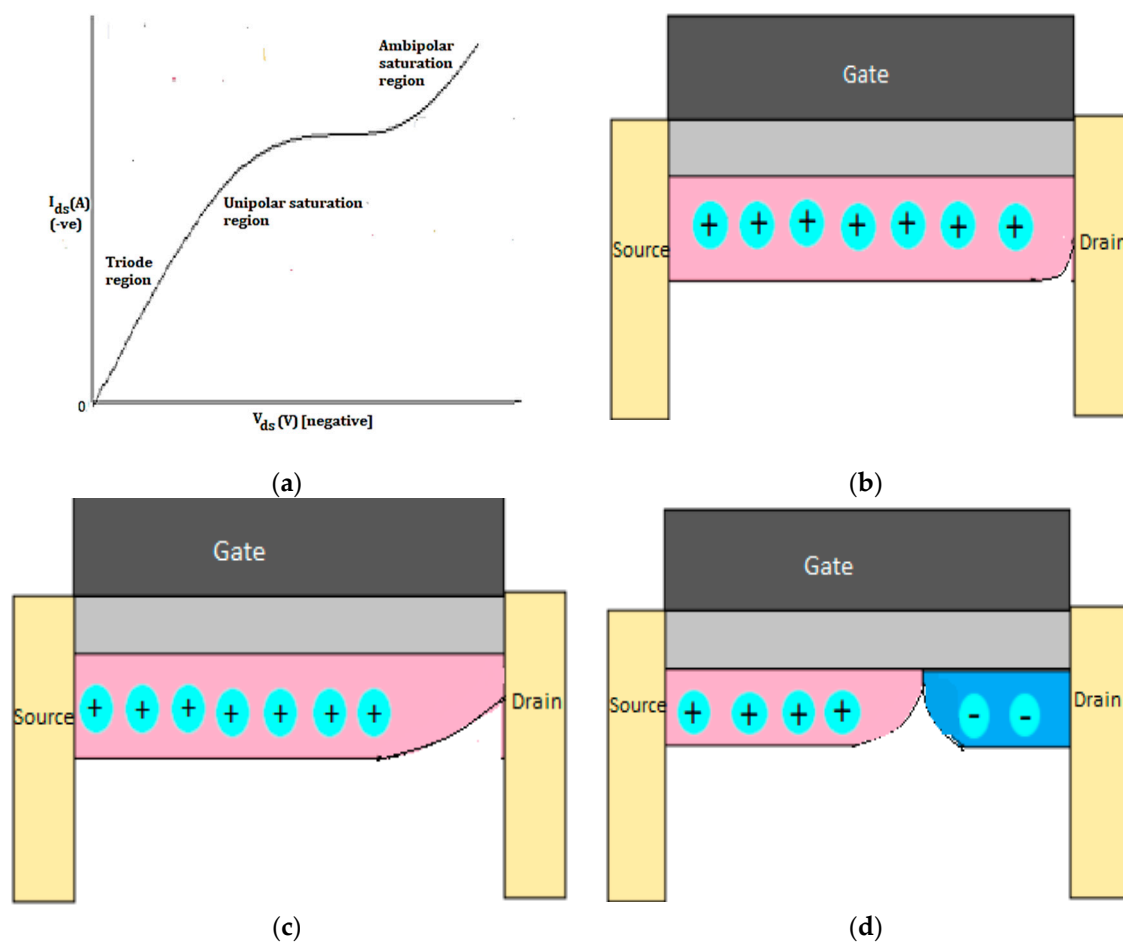


Figure 3. Diagrammatic representation of the charge flow in graphene field effect transistor. (a) I-V curve of transistor. (b) Triode region: Flow of holes and a minimum charge density point started to form at the drain end. (c) Unipolar saturation region: There is a pinching at the drain terminal. (d) Ambipolar region: Graphene channel illustrating both holes’ and electrons’ transport.

In the triode region, the charge carriers (either holes or electrons) between the source and the drain ends generate drain current [29,30]:

$$I_{ds} = -WQ(x)V_E(x). \tag{9}$$

Here, W is the width of the channel and $V_E(x)$ is the drift velocity of the charge carrier. The charge carrier experiences a saturation velocity due to the effective electrical field between drain and source terminal. The drift velocity is formulated by $V_E = \frac{\mu E}{1 + \frac{\mu E}{V_{sat}}}$ [31].

Here, E is the electric field between the drain and the source terminal, μ is the mobility of the charge carrier, and saturation velocity is $V_{sat} = \mu F_C$, where F_C is the critical electric field. In the triode region of the transistor, drain current is directly proportional to drain–source voltage. The electrical voltage in the graphene channel can be written as $V(0) = I_{ds}R_c$ and $V(L) = V_{ds} - I_{ds}R_c$ where R_s is a series resistance at both drain and source ends, respectively, and L is the active length of the graphene channel. The drain current of the triode region can be obtained by applying the Boltzmann equation and integrating Equation (9) along channel length [32]:

$$I_d = \frac{WV_c\mu_0}{2LC_{top}(V_{ds} - 2I_dR_s + V_c)} \times [Q(L)^2 - Q(0)^2], \quad (10)$$

where $Q(L) = -C_{top}(V_{gth} - I_dR_s - V_{ds})$ and $Q(0) = -C_{top}(V_{gth} + I_dR_s)$. Here $V_{gth} = V_{gs} - V_0$ and V_0 can be found from Equation (5). One can derive a simplified drain current Equation (11) by substituting the above values in Equation (10):

$$I_{ds} = \frac{1}{4R_s} [V_{ds} - V_c + \beta \left(V_0 - \frac{V_{ds}}{2} \right) - \sqrt{(V_{ds} - V_c + \beta \left(V_0 - \frac{V_{ds}}{2} \right))^2 - 4V_cV_{ds}}] \quad (11)$$

where $\beta = 2V_{sat}WC_{top}R_s$ and $V_c = \frac{V_{sat}L}{\mu}$.

For the unipolar saturation region, there is a minimum charge density point at the terminal of drain that produces a saturation region. At this point, change of current with respect to voltage is $\frac{\partial I_{ds}}{\partial V_{ds}} = 0$. At the beginning of the first saturation region, the drain-to-source voltage can be defined as

$$V_{ds-sat1} = \frac{2\beta V_{gth}}{1 + \beta} + \frac{1 - \beta}{(1 + \beta)^2} \left[V_c - \sqrt{V_c^2 - 2(1 + \beta)V_cV_{gth}} \right]. \quad (12)$$

After substituting the value of this saturation voltage into drain current in Equation (11), the derivation yields

$$I_{ds-sat} = \frac{\beta}{R_s(1 + \beta)^2} [-V_c + (1 + \beta)V_{gth} + \sqrt{V_c^2 - 2(1 + \beta)V_cV_{gth}}]. \quad (13)$$

From Figure 3a we can depict that the saturation current I_{ds-sat} , which maintains a continual progression through this region. Graphene channel experiences a saturation voltage $V_{ds-sat1}$ at the drain terminal but it may not introduce a charge neutrality point. Considering a direct continuation of charge between $V_{ds-sat1}$ and V_{gth} , the depletion charge between these two voltages will be $Q_{dp} = -\frac{C_{top}}{2} \left(|V_{gth} - V_{ds-sat1}| \right)$, where $V_{gth} = V_{gs} - V_0$. To eliminate this depletion charge, Q_{dep} , $V_{ds-sat2}$ generates and indicates the finishing point of unipolar saturation region. At this moment, the charge between $V_{ds-sat1}$ and $V_{ds-sat2}$ is $-C_{top}(V_{ds-sat1} - V_{ds-sat2})$, which is similar to Q_{dep} . Therefore, the secondary terminal saturation voltage in this region can be formulated as $V_{ds-sat2} = V_{ds-sat1} - \frac{1}{2} \left(|V_{gth} - V_{ds-sat1}| \right)$ [20]. This point introduces a pinch-off region at the drain terminal, which indicates a minimum carrier density. Pinch-off region in the drain current is shown by Figure 3a,c.

From Figure 3b,c, it can be understood that triode and unipolar saturation regions exhibit unipolar charge carrier and that is by holes. Afterwards, an ambipolar region is introduced, where carrier transportation is both by holes and electrons. Further increase in drain-to-source voltage pushes the minimum carrier density point at the pinch-off region toward the inside, i.e., this squeezed portion comes close to the source end. In this way, electrons get scope to enter into the channel, as indicated in Figure 3d. Therefore, this region becomes a complete package of holes and electrons running from source and drain terminals, respectively. For the mobility of the electrons there is no drained region between pinch-off

and drain terminal. This phenomenon ultimately reaches to a concept that explains the zero bandgap theory in two-dimensional bilayer graphene. The voltage and charge accumulated at the drain terminal is $V(L) = V_{ds}$ and $Q(L) = -C_{top}(V_{gs} - V(L) - V_o)$, respectively. Additional charge that is introduced can be formulated as $Q_d = Q(L) - Q(L')$ where $Q_d = -C_{top}(V_{ds} - V_{ds-sat2})$ and μ_n is the mobility of the opposite charge carriers. We can derive $I_{disp} = -\frac{W\mu_n Q_d^2}{2L(C_{top})}$ by applying integration on $Q(x) = -C_{top}(V_{gs} - V(x) - V_o)$ using $\frac{\partial Q_d}{\partial V_d} = -C_{top}$ [26]. As a result, the saturation displacement current is obtained

$$I_{disp} = -\frac{W}{2L}\mu_n(C_{top})V_{ds-sat2}^2\left(\frac{V_{ds}}{V_{ds-sat2}} - 1\right)^2. \quad (14)$$

The saturation drain current at the unipolar saturation region due to depletion charge Q_d and displacement current from additional charges in ambipolar region result in a total current flow in the graphene channel, $I_{ds} = I_{ds-sat} + I_{disp}$.

2.4. Calculation of Transconductance and Transit Frequency

The transconductance (g_m) is a significant parameter for understanding the RF performance of GFET. Generally, high g_m is desirable for high intrinsic gain and cutoff frequency. The g_m can be extracted from transfer characteristics ($I_d - V_{gs}$) of GFET, which means change of drain current with a small change of gate voltage V_{gs} as $g_m = \frac{dI_d}{dV_{gs}}$ Where $V_{ds} = \text{constant}$. Here, the g_m can be calculated by the approximation that the drain-to-source resistance is zero. By taking differentiation of saturation current with respect to voltage gate voltage, transconductance at saturation can be obtained as:

$$g_m^{sat} = \frac{\beta}{R_s(1+\beta)} \left[1 - 1/\sqrt{1 - 2(1+\beta) \times (V_{gth}/V_c)} \right]. \quad (15)$$

Intrinsic cutoff frequency ($f_{T,int}$) is another important parameter to characterize the GFET RF performance. The intrinsic cutoff frequency ($f_{T,int}$) of a transistor is determined by charge carrier transit time across the channel length (L gate). The intrinsic cutoff frequency [33] can be deduced by:

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \quad (16)$$

3. Results and Discussion

Performance of the graphene film as a flexible GFET was calibrated and analyzed. The surface potential and quantum capacitance as a function of gate voltage were investigated. The output and transfer characteristics were obtained. The contribution of high transit frequency as a function of gate voltage and channel length dependence was also found and discussed. Moreover, transconductance and threshold voltage dependence on gate voltages was clarified. The surface potential was expressed as a function of the gate-source voltage and simulated the quantum capacitance as a function of surface potential by using the following data: Top-gate dielectric constant 16.0 and back-gate dielectric constant 3.9 were considered. Herein, the device threshold voltage was considered. The top gate source voltage at the Dirac point V_{gs}^o and back gate source voltage at the Dirac point V_{bs}^o were taken as 1.45 V and 2.7 V, respectively. Back gate oxide layer thickness was taken as 285 nm. Channel series resistance was taken as 850 Ω . Here, surface mobility and mobility of alternative carriers were 700 and 120, respectively. The channel length and channel width were assumed as 440 nm and 1 μm , respectively. The top-gate oxide-layer thickness was taken as 15 nm. The critical electrical field was considered as 4.5 KV/cm.

3.1. Top-Gate-to-Source Voltage Dependence on Quantum Capacitance and Surface Potential

The graphical presentation of gate-to-source voltage with quantum capacitance and surface potential is shown in Figure 4. It was found that a V-shaped curve where the maximum value of quantum capacitance occurred at 0.13 Fm^{-2} at -3 V and at 3 V , respectively. The minimum quantum capacitance was obtained as 0.01 Fm^{-2} at $V = 0$. The top-gate and back-gate dielectric constants were taken as 16.0 and 3.9, respectively. Increase of dielectric constant meant increase in the charge accumulation in the channel. Therefore, the capacitance was automatically increased for a particular fractional change in potential. Increase in charge carrier concentration meant high on-current as well as high off-current but an increase in on/off ratio.

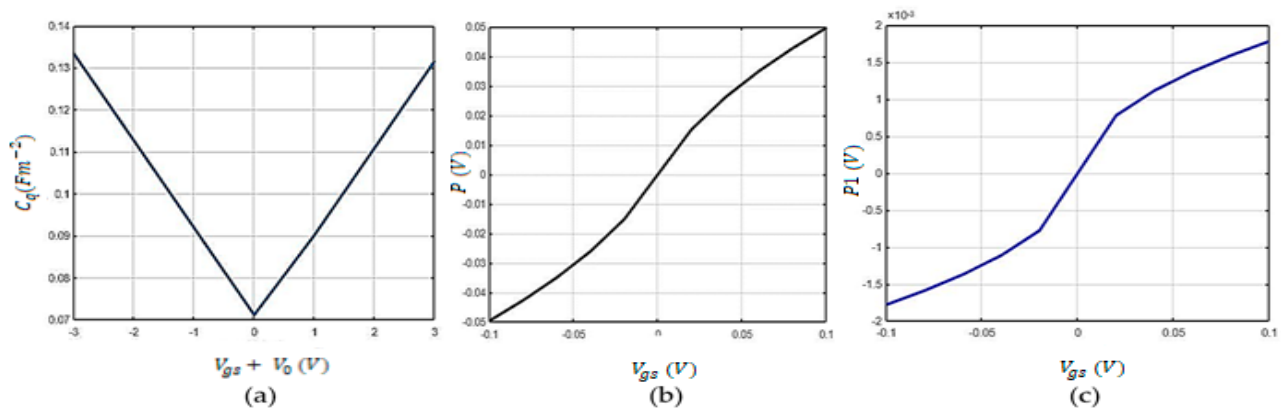


Figure 4. Graphical representation of gate-to-source voltage with quantum capacitance and surface potential as: (a) quantum capacitance as a function of top-gate-to-source voltage and (b) surface potential P (V) vs. top-gate-to-source voltage of a graphene field effect transistor (FET) from equation of surface potential [21]. (c) Surface potential $P1$ (V) vs. top-gate-to-source voltage V_{gs} (V) from Laitinen equation of Fermi level shift [28].

According to the calculation of the surface potential in Section 2, it was dependent on the gate voltage, and the plot in Figure 4b confirms it. Actually, the surface potential p (v) in Figure 4b is the potential difference between the channel and the source terminal. For each value of quantum capacitance, surface potential vs. gate voltage was obtained self-consistently. At $V_{gs} = 0$, surface potential was also zero. At minimum gate voltage $V_{gs} = -0.1 \text{ V}$, surface potential $P = -0.05 \text{ V}$ was taken. At maximum gate voltage $V_{gs} = +0.1 \text{ V}$, surface potential $P = 0.05 \text{ V}$ was taken, i.e., characteristics were also anti-symmetrical. Fermi level is related to surface potential by the relation $E_f = qp$ where E_f is Fermi level, q is the quantum capacitance, and P is the surface potential. Positive value of surface potential indicates that the Fermi level is in the conduction band, negative value indicates that the Fermi level is in the valence band, and a zero value indicates a charge neutrality point.

Figure 4c confirms the theory represented by the Laitinen equation of Fermi level energy shift in the suspended part of graphene [28]. At the same time, it shows resemblance with Figure 4b.

3.2. Relationship between Drain Current and Voltages

The curve in which the relationship between drain current and drain voltage has been represented gives the output response of the device, as illustrated in Section 2 theoretically in Figure 4a, which shows the output characteristics of this GFET for electron conduction. Through application of a positive gate voltage and a positive drain voltage, it provides current flow only when V_{gs} is higher than the device threshold voltage.

The behavior for electron conduction is shown in Figure 5a where top-gate voltages $V_{gs} = 0 \text{ V}, 0.5 \text{ V}, 1 \text{ V}, 1.5 \text{ V}$ and 2 V , $V_{bs} = +40 \text{ V}$, $R_c = 850 \Omega$, $\mu = 700 \frac{\text{cm}^2}{\text{V}} \times s$, $E_c = 4.5 \text{ KV/cm}$, and $\mu_n = 120 \frac{\text{cm}^2}{\text{V}} \times s$ are estimated, respectively. The output characteristics showed a linear

region, a weak saturation region, and, in some cases, a second linear region. The value of I_d is 0.00121 A at saturation region. Good current saturation and disappearance of second linear region were observed on output characteristics for higher V_{gs} . The maximum on-state current of 1.21 mA was obtained for $V_{gs} = 2$ V and $V_{ds} = 1$ V.

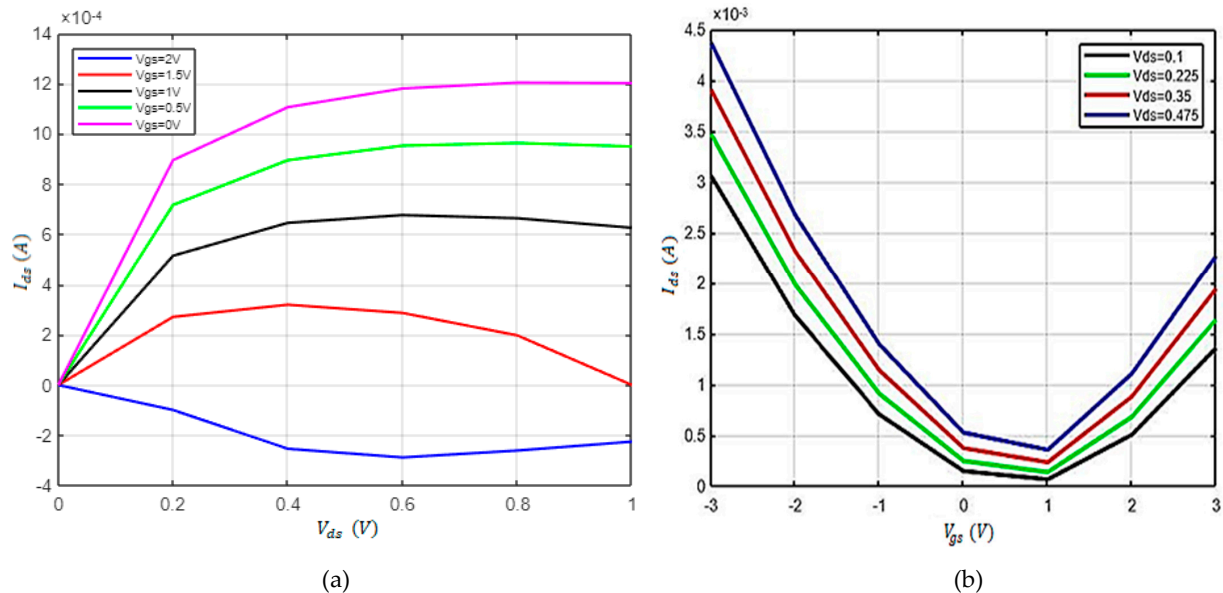


Figure 5. Graphical representation of drain-to-source and gate-to-source voltages with drain current as: (a) output characteristics of GFET and (b) drain current versus top-gate voltage.

In Figure 5b, the drain current shows a V-shaped curve with respect to the top-gate-to-source voltage. It represents the transfer characteristics of a particular device. The characteristics were plotted for a transistor with $V_{bs} = +40$ V, $R_c = 850 \Omega$, $\mu = 700 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$, and $\mu_n = 120 \frac{\text{cm}^2}{\text{V}\cdot\text{s}}$ with a V_{ds} of 0.1 V, 0.225 V, 0.35 V, and 0.475 V for electron conduction. $V_{gs} = -3$ V, -2 V, -2 V, 0 V, 1 V, 2 V, and 3 V were taken, respectively. For different V_{ds} , where ambipolar conduction was clearly distinguished by a Dirac point, there was an asymmetry in p-type and n-type conduction in transfer characteristics. The Dirac point represents the vanishing point of density of states but there is a minimum conductance unlike other semiconductors. The position of Dirac point depends on several factors: the difference between the work functions of the gate material and graphene, the type and density of the charges at the top and bottom of the interfaces of the channel, and the amount of doping of the graphene. The value of residual charge at the Dirac point increases with V_{ds} as the channel potential depends not only on the V_{gs} but also on the V_{ds} .

3.3. Characteristics of Transconductance and Transit Frequency

The output conductance g_m is the change in the drain current with a small change in the gate source voltage while maintaining the drain source voltage constant. In Figure 6a, g_m is shown for a range of V_{gs} with $V_{bs} = 40$ V. Length and width of graphene channel was taken as 440 nm and 1 μm , respectively. Here, $V_{TH,0} \sim 0$ V, $C_{Top} = 3.6 \times \frac{10^{-3}F}{\text{m}^2}$, and $\mu = 7000 \text{ cm}^2$ were considered. It is interesting to notice that output characteristics displayed a linear region for low voltage bias (V_{gsi}) and a saturation region for high voltage bias. The g_m dropped substantially at large V_{gsi} biasing voltage, mainly due to the effect of V_{sat} . As per the equation presented in Section 2.3, there is an inverse relationship between transconductance and gate source voltage. Therefore, the best g_m performance was actually achieved at low effective gate-to-source overdrive voltage V_{eff} , where $V_{eff} = V_{gsi} + V_{TH,0}$. The Figure 6b shows the estimation of transit frequency at which the current gain of the

device drops to one, and it is a measure of its high-speed and bandwidth capabilities. Here, $V_{dsi} = 0.1$ V, 0.3 V and 0.5 V was taken.

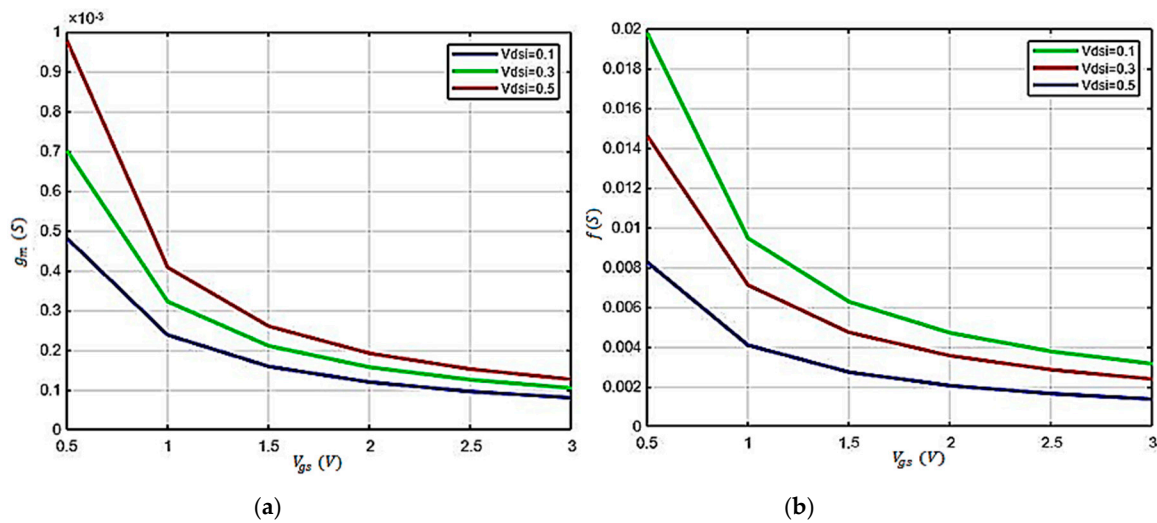


Figure 6. Graphical representation of the drain transconductance and transit frequency. (a) Transconductance as a function of gate voltage of graphene field effect transistor (GFET). (b) Transit frequency as a function of gate-to-source voltage.

3.4. Threshold Voltage Dependence on Back-Gate-to-Source Voltage

In the case of the plot, as shown in Figure 7, SiO_2 was used as dielectric. For a given back gate voltage (V_{bs}), the threshold voltage (V_o) was dependent on the device capacitances. Model parameters used are estimated in Table 1. For the test case shown in Figure 6, a good fit against experimental data was attained with top gate capacitance $C_g = 200$ nF \cdot cm $^{-2}$ and back gate capacitance $C_b = 12$ nF \cdot cm $^{-2}$, respectively. It was reported that the threshold voltage V_o against V_{bs} was a straight line graph with the slope being the ratio of the gate capacitances, as illustrated in Section 2.

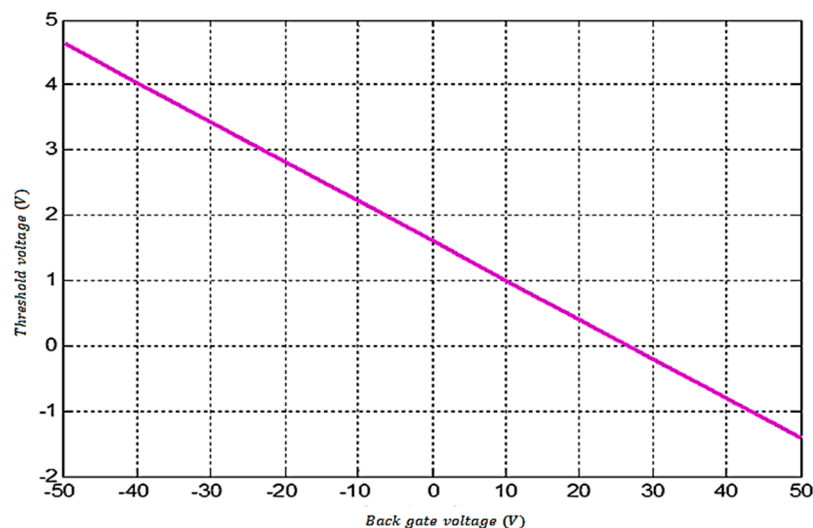


Figure 7. Graphical representation of threshold voltage dependence on back-gate-to-source voltage using silicon dioxide as dielectric.

Table 1. Model parameters for bilayer graphene field effect transistor (FET).

Model Parameter	Test Value	Estimated Value
L (μm)	1	440
W (μm)	2.1	1
t_{ox} (nm)	15	15
E_C (KV/cm)	4.5	4.5
K_1	16.0	16.0
K_2	3.9	3.9
V_{gs}^0 (V)	1.45	1.45
V_{bs}^0 (V)	2.7	2.7
$\left(\frac{\text{cm}^2}{\text{V}} \cdot \text{s}\right)$	600	700
μ_n ($\frac{\text{cm}^2}{\text{V}} \cdot \text{s}$)	120	120
R_C (Ω)	850	850
V_{bs} (V)	+40	+40

4. Proposed Capacitive Model of Multilayer Graphene FET

In Figure 8, four-layered and six-layered capacitive models are proposed. More extension of graphene channel can be done in a similar way. This is the equivalent demonstration of multilayer graphene FET. The layers are individually represented by quantum capacitance C_q . There is an interlayer capacitance C_o between the gaps of each of the channels. Further studies for multilayer channel can be done based on the formulae presented in Section 2 and simulating the properties using MATLAB.

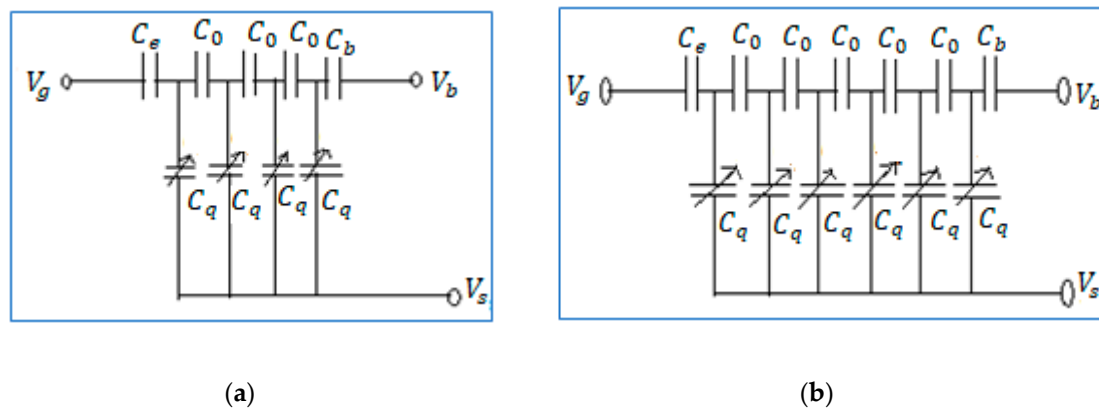


Figure 8. Equivalent capacitance model: (a) graphene channel with four layers, (b) graphene channel with six layers.

5. Conclusions

This paper presented a theoretical model for single- and bilayer graphene channel. Later on, practical analysis of a dual-gate bilayer graphene FET was done utilizing MATLAB software. It considered the approximation of equality of mobility of electrons. Better output characteristics, transfer function, and transconductance behavior of GFET than FETs of other conventional semiconductors were obtained. The quantum capacitance as a function of top-gate-to-source voltage and surface potential with variation of gate bias was depicted. The minimum capacitance of 0.01 Fm^{-2} was obtained at the Dirac point where voltage is zero. When gate bias was negative, it gained negative value with a zero at zero gate bias. It was also found that when gate voltage was positive, it increased from zero value to source positive value. At minimum and maximum gate voltage, the surface potential was -0.05 V and $+0.05 \text{ V}$, respectively. A set of output characteristics for different gate voltages was obtained. The drain current increased linearly then became saturated. The maximum 1.18 mA on state current was found. The transfer characteristics of the proposed model showed that, when gate voltage increased from a negative value, drain current reduced,

at zero gate bias and over some voltages it became partially saturated, and then with the positive values' output current tended to rise again. The transconductance estimation as a function of gate voltage for different drain-to-source voltages depicted proportional relationship; however, with the increase of gate voltage this value tended to fall. The transit frequency response as a function of gate voltage was represented whereas with the decrease of channel length the increment of transit frequency was obtained. The threshold voltage dependence on back gate source voltage for different dielectrics depicted that there was an inverse relationship between the two. Finally, equivalent capacitive model for multilayer graphene FET was proposed. The findings can be extended, including the following. (1) Extensive investigation can be done for multilayer graphene FET using MATLAB. (2) Contact resistance effect can be included for obtaining accurate performance. So this work can be extended for different contact metal stacks, metal alloys etc. (3) Buffer layer can be used to improve the device performance. Since phonon and surface roughness scattering reduces the mobility significantly, the buffer layer could make a good interface with reduced remote phonon scattering, which results in higher mobility.

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