

Article

Flyback Converter for Solid-State Lighting Applications with Partial Energy Processing

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Abstract: The main contribution of this paper is to show a new AC/DC converter based on the rearrangement of the flyback converter. The proposed circuit only manages part of the energy and the rest is delivered directly from the source to the load. Therefore, with the new topology, the efficiency is increased, and the stress of the components is reduced. The rearrangement consist of the secondary of the flyback is placed in parallel with the load, and this arrangement is connected in series with the primary side and the rectified voltage source. The re-arranged flyback is only a reductive topology and with no magnetic isolation. It was studied as a power supply for LEDs. A low frequency averaged analysis (LFAA) was used to determine the behavior of the proposed circuit and an equivalent circuit much easier to analyze was obtained. To validate the theoretical analysis, a design methodology was developed for the re-arranged flyback converter. The designed circuit was implemented in a 10 W prototype. Experimental results showed that the converter has a $THDi = 21.7\%$ and a $PF = 0.9686$.

Keywords: lighting; light-emitting diodes; LED driver; electrolytic-capacitor-less converter; partial power processing converters; power factor correction (PFC)



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1. Introduction

Nowadays, LEDs are considered the future of lighting, since they have an increasing demand caused by the long useful life that they have, around 50,000 h [1] and the lighting efficiency they present, which can reach up to 160 lm/W in the laboratory. Power supplies must meet power quality standards, which contemplate total harmonic content ($THDi$) at the input current and power factor (PF) [2]. The guidelines for lighting systems connected to the line are specified in the IEC61000-3-2 class C standard [3].

In general, it is common to find LED power supplies with a power factor correction (PFC) stage, after the bridge of the rectifier diode, to ensure regulatory compliance. The single-stage PFC converter has the advantage of having high efficiency since only one converter processes the total energy.

However, the power supply also must convert the AC power from the main line to the constant power that the LED needs for good performance [4,5], but to achieve this, it is necessary to have an element that can store a large amount of pulsing energy. A large capacitor could solve this problem; however, large capacitance values are generally handled in electrolytic capacitors, which generate a bottleneck due to their short lifespan, compared to LEDs, so it is recommended to avoid their use [6–8].

To avoid the use of the electrolytic capacitor, another converter is usually added, in series or parallel to try to reduce the low-frequency current ripple that is supplied to the LED and operate with a low capacitance value. This solution generates a two-stage converter; the first with the task of the PFC and the second that must compensate for the low-frequency ripple; this latter maintains the advantage of a fast control action [9,10]. This allows the use of film capacitors that have a lifespan similar to that of LEDs [1,7,8]. However, the overall efficiency of the lighting system is decreased and therefore reduces the ratio lumens per watt (lm/W). This is because the total energy of the system is processed twice.

Some works seek alternative solutions through other techniques, such as integrated converters [11–18], harmonic injection [19–21], ripple cancellation and ripple ports [17,22–31], and power decoupling techniques were also analyzed [32–35].

All of them have a PFC converter as the first stage and make some adjustments in the operation of the circuit to change the energy processing and eliminate the low-frequency ripple current. In these converters, the energy is not processed twice, since they follow the principle of reduced redundant energy processing (R^2P^2) [18,22,36–38]. They prevent the energy processed by one converter from being completely processed by another converter. Some of these jobs are called 1.5-stage converters by themselves.

In this work, a converter is presented that does not seek to solve the output capacitor problem. However, the principle of reduced redundant power processing (R^2P^2) is taken further and created a 0.5-stage converter, which can improve the efficiency of any PFC converter and still comply with corresponding regulations.

The proposed converter is a re-arranged variation of the flyback converter; placing the secondary of the flyback in parallel with the load and this arrangement is connected in series with the primary side and the rectified voltage source. This configuration allows part of the energy from the source to pass directly to the load, and another part to be processed by the rearranged flyback converter, thus increasing the efficiency of the entire system. To analyze the proposed circuit, a low frequency averaged analysis (LFAA) was carried out, which resulted in an equivalent circuit that was very easy to evaluate and thus determine its behavior and design method. As the flyback converter is an isolated topology, it is possible to use some other of the aforementioned methods, such as ripple ports, to be able to eliminate low-frequency ripple current in the load. This paper is organized as follows: Section 2 presents and explains the operation and mathematical analysis of the converter. Section 3 focuses on converter design and simulation in Spice. Section 4 shows the results obtained, and finally, in Section 5, the main conclusions of this document are presented.

2. Mathematical Analysis of the Proposed Circuit

The interface between the AC power supply and an LED load is called online LED driver, the driver should have a power factor greater than 0.9 according to the U.S. Energy Star program [2]. The LED drivers must also comply with the current harmonics level specified in IEC 61000-3-2 Class C [3]. Therefore, a Power Factor Converter (PFC) should be used to meet the usual requirements for an LED power supply. In Figure 1 the proposed topology is shown. The converter consists of a variation of the flyback converter in which the secondary stage is connected in parallel with the LED lamp and these in turn in series with the primary stage.

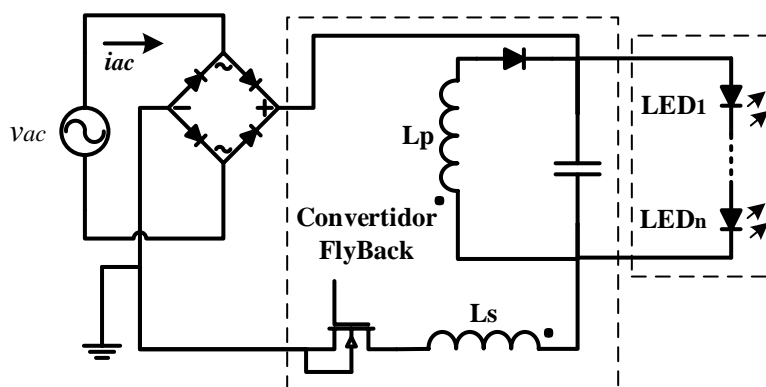


Figure 1. Proposed topology: Rearranged flyback converter, with primary and secondary in series.

In order to carry out the analysis of the rearranged flyback converter, a low-frequency average analysis (LFAA) was used; This is used to know in a general way if a topology complies with the corresponding regulations, knowing its efficiency, and evaluating its feasibility of implementation. The LFAA model the behavior of the flyback converter at the frequency line. At this frequency and due to the discontinues conduction mode (DCM) of the flyback converter, the primary side can be represented as a loss-free resistance (R_F), this resistance represents the average power delivered to the primary side of the flyback converter (P_{Fi}), the energy “consumed” by this resistance is transferred to the secondary side of the flyback converter that is modeled as a direct current voltage source (V_F), as shown in Figure 2.

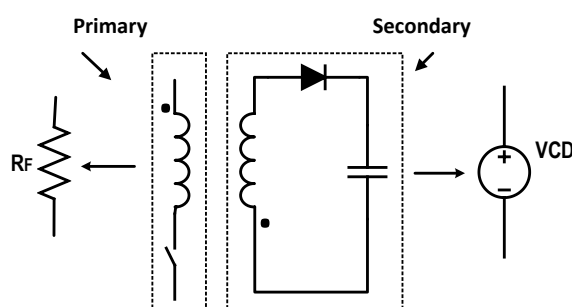


Figure 2. Flyback model in DCM for the LFAA.

On the LED side, it can be modeled as a series direct DC voltage source with a resistor, as shown in Figure 3.

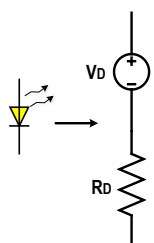


Figure 3. LED model.

Figure 4 shows the equivalent low-frequency scheme corresponding to the circuit proposed in Figure 1. Where: v_r is the rectified Voltage, i_r is the rectified Current, V_F is the average voltage in the secondary of the flyback converter, R_F Loss-free resistance representing the primary of the flyback converter, V_D representing the LED threshold voltage of the LED model, R_D is the resistance of the LED model.

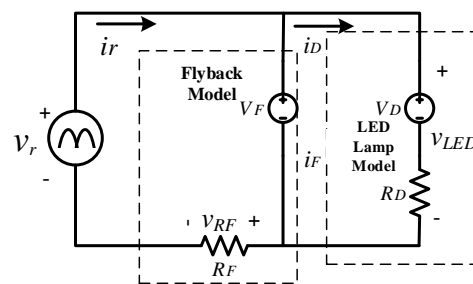


Figure 4. Equivalent circuit for low-frequency analysis.

The loss free resistance is evaluated with the following expression:

$$R_F = \frac{P_{Fi}}{I_{Rrms}^2} = \frac{P_{Fi}}{\frac{2}{T} \int_0^{\frac{T}{2}} i_r^2 dt} \tag{1}$$

where I_{Rrms} is the RMS value of i_r .

2.1. Analysis of the Power Factor (PF) and the Current Total Harmonic Distortion (THDi) Using LAAA

In Figure 4, it is observed that the LED is powered by the voltage source V_F , it is interesting to obtain the expression of i_r . applying Kirchoff's voltage law to the scheme we obtain:

$$v_{LED} = V_F = V_D + i_D \cdot R_D \tag{2}$$

$$i_r = \frac{v_r - V_F}{R_F} \tag{3}$$

Additionally, the following observations were made:

1. The topology is reductive, so it is always true that $V_F < V_r$, where V_r is the peak voltage of $v_r(t)$, as shown in (4).
2. There will be current flow through R_F if $v_r > V_F$, when $v_r < V_F$ the current $i_r(t) = 0$, as V_r approaches V_F there will be very long death times. Therefore, the i_r waveform will be the same as i_{ac} at $T/2$ as shown in Figure 5.

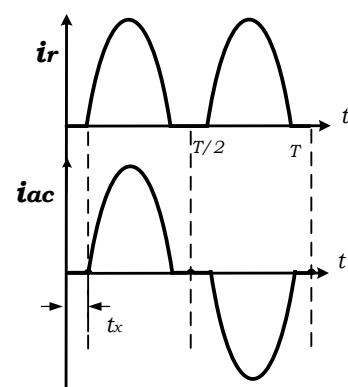


Figure 5. Current waveforms of the topology i_{ac} and i_r .

$$v_r = V_r |\sin \omega t| \tag{4}$$

where t_x is a constant that represents the dead time, which is given by:

$$t_x = \frac{\sin^{-1}\left(\frac{V_F}{V_r}\right)}{2\pi f} = \frac{\sin^{-1}(m)}{\omega} \tag{5}$$

where $m = V_F/V_r$ is the gain of the proposed converter, ω is the angular frequency and f is the line frequency.

In order to calculate the *PF* and *THDi* in the proposed converter, it is necessary to know the harmonics of the input current waveform (i_{ac}), shown in (6). For this, t_x can be used in the integration limits of the calculation of the Fourier coefficients of i_{ac} in (7) and verify if the topology meets the requirements of IEC61000-3-2 class C.

$$i_{ac} = \begin{cases} \frac{V_r \sin(\omega t) - V_F}{R_F} & t_x < t < \frac{T}{2} \\ \frac{V_r \sin(\omega t) + V_F}{R_F} & \frac{T}{2} < t < T - t_x \end{cases} \quad (6)$$

$$i_{ac} = \underbrace{a_0}_{dc} + \underbrace{\sum_{n=1}^{50} (a_n \cos(n\omega t) + b_n \sin(n\omega t))}_{ac} \quad (7)$$

The waveform being analyzed (i_{ac}) is an odd function, therefore there are only odd harmonics. The *THDi* is obtained from (8), where I_1 is the fundamental component that is defined in (9), and I_n is the amplitude of the n -th harmonic that is defined in (10).

$$THD_i = 100 \cdot \sqrt{\sum_{n=3}^{50} \left(\frac{I_n}{I_1}\right)^2} \quad (8)$$

$$I_1 = 2 \cos(\omega t_x) \sin(\omega t_x) - 4m \cos(\omega t_x) - 2\omega t_x + \pi \quad (9)$$

$$I_n = \frac{-4}{n(n-1)(n+1)} \sin\left(\frac{n\pi}{2}\right)^2 \left(\begin{matrix} m \cdot (n^2 - 1) \cos(n\omega t_x) + \\ \left(\frac{n^2+n}{2}\right) \sin((n-1)\omega t_x) - \\ \left(\frac{n^2-n}{2}\right) \sin((n+1)\omega t_x) \end{matrix} \right) \quad (10)$$

Returning to (8) and assuming the main voltage is sinusoidal the *PF* is obtained by:

$$PF = \frac{1}{\sqrt{1 + \frac{THD_i^2}{100^2}}} \quad (11)$$

Figure 6 shows the plot of (8), assuming $THD_i \leq 32\%$, it can be seen that the gain m can vary from 0 to 0.46. If $m > 0.46$ the *THDi* will be very high and the power factor *PF* very low.

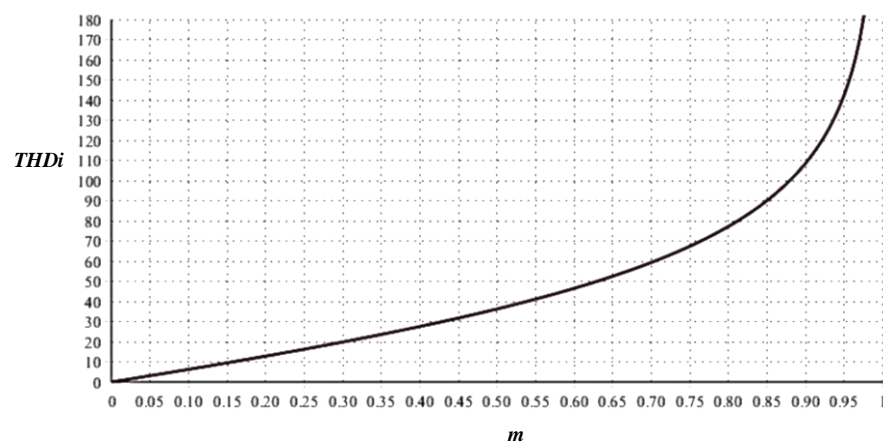


Figure 6. *THDi* of topology vs gain (m).

Regarding the requirements of the IEC61000-3-2, Figure 7 shows the curves for the odd harmonics from $n = 3$ to $n = 15$, it is observed that the topology is limited in a range of $0 < m < 0.41$.

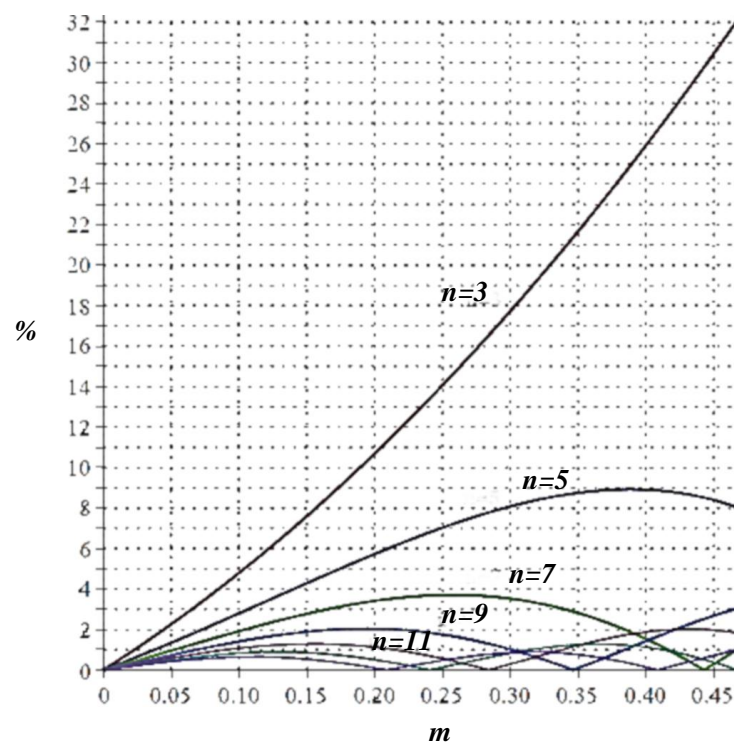


Figure 7. Curves of each harmonic of the topology vs the gain (m).

From Figure 8, where (11) is plotted, it can be seen that the topology meets the requirements of a $PF > 90$ without a problem in a range of $0 < m < 0.41$.

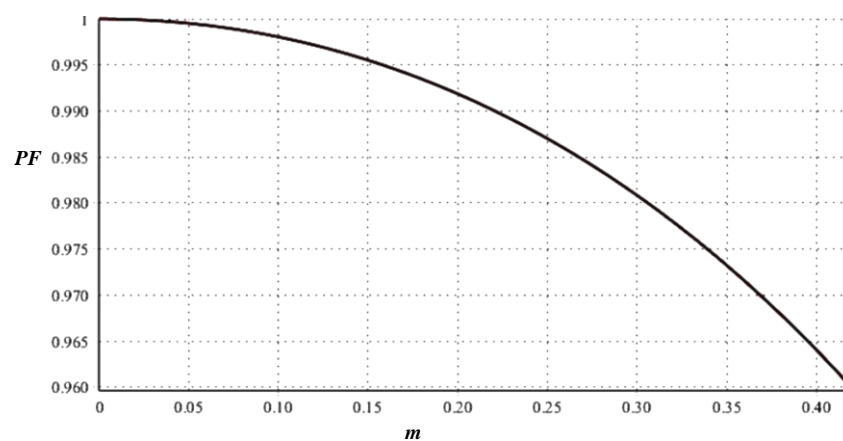


Figure 8. PF of the topology vs the gain (m).

From this section it is concluded that the proposed topology complies with all applicable standards in the range of $0 < m < 0.41$.

2.2. Analysis of the Power Flow in the Converter

In order to analyze the power flow in the proposed converter the following concepts are defined in Table 1.

Figure 9 shows the power flow diagram of a conventional flyback compared with the proposed rearranged flyback. In this diagram, it is easier to understand the operation of the proposed converter, in which it is observed as part of the input power P_i is supplied directly to the load, while the other fraction is processed by the P_{Fi} flyback converter. Therefore, the total efficiency concerning the conventional flyback will be improved.

Table 1. Power flow concepts.

Symbol	Description	Definition
P_L	Average power consumed by the load	$P_L = \frac{1}{T} \int_0^T v_{LED} i_d dt$ (12)
P_i	Average power delivered by the main source	$P_i = \frac{1}{T} \int_0^T v_r i_r dt$ (13)
P_{Fi}	Average power delivered to the primary side of the flyback converter	$P_{Fi} = \frac{1}{T} \int_0^T v_{RF} i_r dt$ (14)
P_{Fo}	Average power delivered by the secondary side of the flyback converter	$P_{Fo} = \frac{1}{T} \int_0^T V_{Fi} i_r dt$ (15)
Q	Ratio between the power processed by the flyback converter and the input power of the proposed converter	$Q = \frac{P_{Fi}}{P_i}$ (16)
η	Efficiency of the proposed converter	$\eta = \frac{P_L}{P_i}$ (17)
η_F	Efficiency of the flyback	$\eta_F = \frac{P_{Fo}}{P_{Fi}}$ (18)

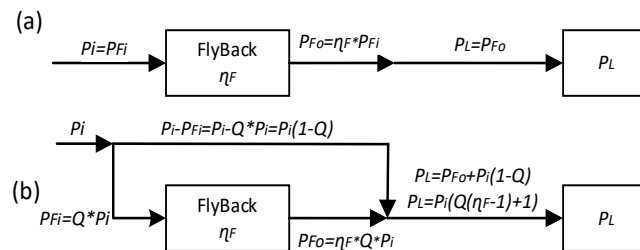


Figure 9. Power flow diagrams, (a) conventional flyback and (b) proposed rearranged flyback. P_i is the input power to the converter.

The percentage of power processed by the flyback is called the constant Q . The range of Q must be $0 < Q < 1$, if Q is greater than 1 there is no point in implementing the topology since instead of having benefits, low efficiency and greater electrical size would be obtained concerning an isolated basic flyback.

According to Figure 9 the total efficiency η of the converter will be:

$$\eta = \frac{P_L}{P_i} = Q(\eta_F - 1) + 1 \tag{19}$$

This equation was plotted in Figure 10 assuming an arbitrary value for the flyback efficiency $\eta_F = 0.9$. As can be seen in this figure, regardless of the Q value, the efficiency of the proposed converter will always be greater than the efficiency of a conventional flyback. Total efficiency will increase as the flyback converter processes less energy.

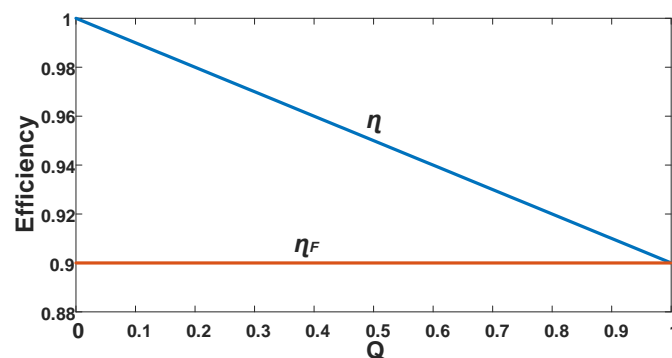


Figure 10. Estimated efficiency of the proposed converter vs Q .

Substituting (3) and (4) in the expressions of Table 1 with the definition of m :

$$P_{Fo} = \frac{V_F}{T} \int_{t_x}^{T/2-t_x} i_r dt = \frac{mV_r^2(2\omega m t_x - \pi m + 2 \cos(\omega t_x))}{R_F \pi} \tag{20}$$

$$P_{Fi} = \frac{R_F}{T} \int_{t_x}^{T/2-t_x} i_r^2 dt = \frac{V_r^2(2 \cos(\omega t_x)[\sin(\omega t_x) - 4m \cos(\omega t_x)] + (\pi - 2\omega t_x)(1 + 2m^2))}{R_F \pi} \tag{21}$$

$$P_i = \frac{1}{T} \int_{t_x}^{T/2-t_x} v_r i_r dt = \frac{V_r^2(2 \cos(\omega t_x) \sin(\omega t_x) - 4m \cos(\omega t_x) - \omega t_x + \pi)}{R_F \pi} \tag{22}$$

$$Q = \frac{-2\omega m^2 t_x + \pi m^2 - 2m \cos(\omega t_x)}{\cos(\omega t_x) \sin(\omega t_x) - 2m \cos(\omega t_x) - \omega t_x + \pi/2} + 1 \tag{23}$$

$$I_{ravg} = \frac{1}{T} \int_{t_x}^{T/2-t_x} i_r dt = \frac{V_r(2\omega m t_x - \pi m + 2 \cos(\omega t_x))}{R_F \pi} \tag{24}$$

In Figure 11, the graph (23) is obtained, in which it is observed that when m increases, Q decreases; this is favorable since the flyback by processing fewer power benefits the total efficiency of the system.

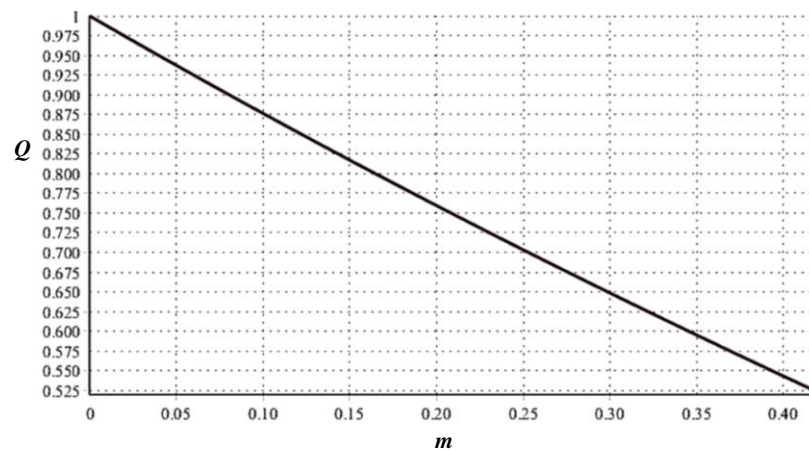


Figure 11. Percentage of power processed by the flyback Q vs Gain m .

3. Design of the Rearranged Flyback

For the implementation of the rearranged flyback converter circuit, LEDs were purchased from the manufacturer Seoul Semiconductor with part number SAW0LH0A. An array of 8 LEDs was made in parallel, which is shown in Figure 14.

The resulting specifications of the LED array are shown in Table 2, which will be used to simulate at low frequency.

Table 2. Technical specifications of the LED test lamp.

V_D	R_D	I_D	V_{LED}	P_L
56 V	28.1 Ω	160 mA	60.5 V	9.68 W

In order to calculate the components of the converter, some design parameters must be proposed, which are shown in Table 3, among them it is worth noting that the flyback dead time is defined in DCM for AC-DC converters [16]. With the values of Table 3, and

the equations previously developed, the necessary values for the implementation of the converter are shown in Table 4.

Table 3. Design parameters proposed.

Parameter	Equation and Value
Line voltage	$v_{ac} = 127 \text{ Vrms}$
Peak voltage	$V_r = 127 \cdot \sqrt{2} \approx 180 \text{ V}$
Proposed flyback efficiency	$\eta_F = 0.95$
Average tension in the secondary	$V_{LED} = V_F = 60.5 \text{ V}$
Proposed duty cycle	$D = 0.405$
Switching frequency	$f_s = 107 \text{ kHz}$
Proposed duty cycle of discharge	$D_{desc} = 0.302$
Proposed voltage ripple	$\%V_{Rip} = 16\%$
EMI capacitor used	$C_{emi} \approx 92 \text{ nF}$

Table 4. Design of the proposed converter.

Parameter	Equation and Value
Gain	$m = \frac{V_F}{V_r} = \frac{60.5\text{V}}{180\text{V}} \approx 0.336$
Dead time of i_r .	$t_x = \frac{\sin^{-1}(m)}{\omega} = 909.26 \mu\text{s}$
THDi	$THD_i = 22.56\%$
PF	$PF = 97.55\%$
Primary winding impedance	$R_F = 971.918 \Omega,$
Primary winding power	$P_{Fi} = 5.904 \text{ W},$
Average input current	$i_{ravg} = 62.41 \text{ mA}$
Electrical Size	$Q = \frac{P_{Fi}}{P_i} = 60.9\%$
Average flyback output power	$P_{Fo} = \eta_F P_i \approx 5.6 \text{ W}$
Average voltage at the primary	$V_{in} = \sqrt{P_{Fi} \cdot R_F} \approx 75.6 \text{ V}$
Average current in the secondary	$I_o = \frac{P_{Fo}}{V_F} \approx 92.65 \text{ mA}$
Flyback converter gain	$M = \frac{V_o + V_{diode}}{V_{in}} = \frac{60.5+1}{75.7} \approx 0.813$
Discontinuity parameter	$k = \sqrt{D_{desc}} \approx 0.248$
Primary inductance	$L_p = \frac{D^2 \cdot V_{in}^2}{2 \cdot P_{Fi} \cdot f_s} \approx 757 \mu\text{H}$
Transformation relation	$N = \frac{D}{M \cdot D_{desc}} \approx 1.659$
Secondary inductance	$L_s = \frac{L_p}{N^2} \approx 278.4 \mu\text{H}$
Capacitor	$C = \frac{P_i}{4 \cdot \pi \cdot 60\text{Hz} \cdot V_F^2 \cdot V_{rip}} \approx 22 \mu\text{F}$
Calculated EMI inductor	$L_{emi} \approx \frac{1}{C_{emi} \cdot (2 \cdot \pi \cdot \frac{f}{10})^2} \approx 2.7 \text{ mH}$

In order to evaluate the proposed circuit before the implementation, a simulation of the circuit was made in Spice. In Figure 12, The schematic is shown, and the results of the simulation are shown in Figure 13.

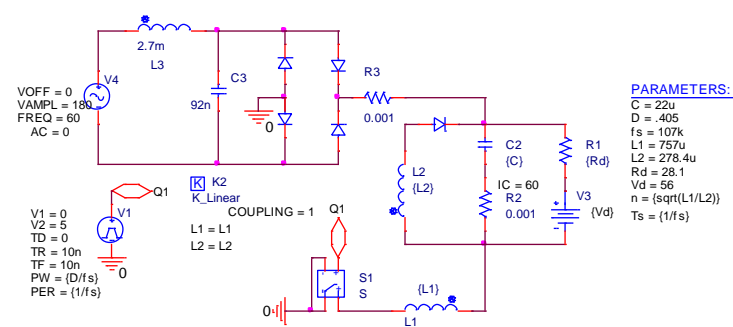


Figure 12. Proposed circuit simulated in spice.

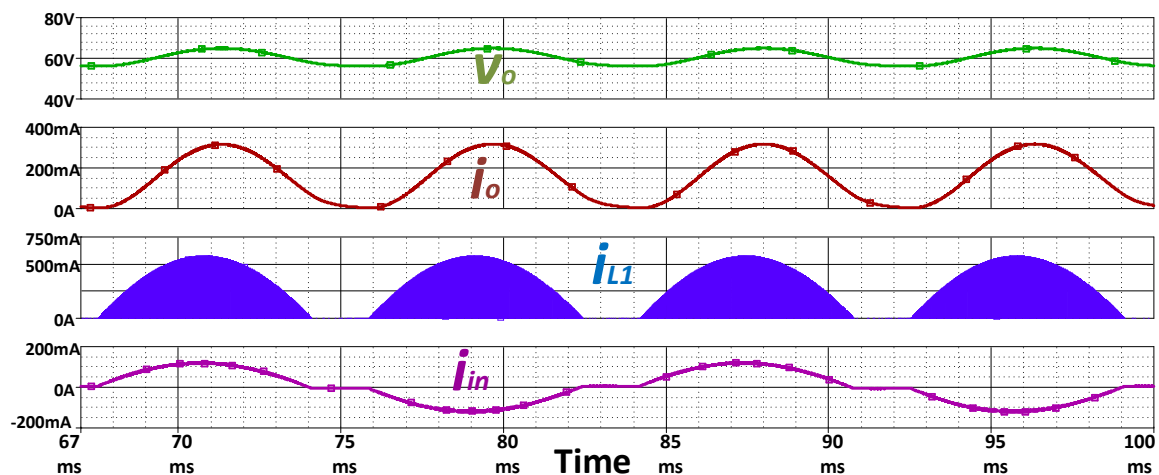


Figure 13. Waveforms resulting from the simulation in Spice. Output voltage (v_o), output current (i_o), current of the primary side (i_{L1}), and input current (i_{in}).

4. Experimental Results

A laboratory prototype has been built to carry out experimental tests and evaluate the performance of the proposed converter. an IR2106 driver and a MOSFET IRF840 were used. The prototype for experimental tests is shown in Figure 14.

Figure 15 shows the main line current and voltage waveforms. As can be seen in this Figure the current waveform shows the death time t_x predicted by the LFAA and this waveform is similar to the theoretical waveform shown in Figure 5.

The $THDi$ of the input waveforms of Figure 15 was measured with the HIOKI model PW3198 power quality analyzer, which is shown in Figure 16, which shows that the $THDi$ is close to 21.7% and the harmonics are within the requirements of the EN 61000-3-2 class C standard. As for the PF obtained in experimental tests with the energy quality meter, it is shown to be 0.9686 in Figure 17.

The instantaneous voltage of the LED lamp obtained in experimental tests is shown in Figure 18. The average voltage applied to the LED was $V_{LED} = 60.5$, the same of the specifications, the voltage ripple obtained was 18.16%. The instantaneous current of the LED lamp obtained in experimental tests is shown in Figure 19. The average current applied to the LED was $I_{LED} = 160.3$ mA, the current ripple obtained was 212%. Finally, in Figure 20 the instantaneous output power in the LED is shown. which shows an average power of $P_o = 10.62$ W.

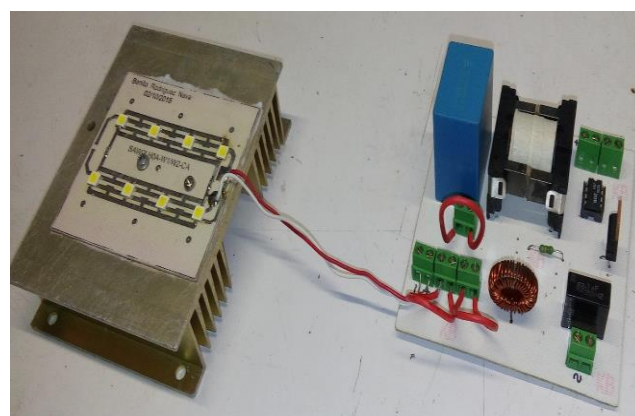


Figure 14. Prototype of the topology for experimental tests.

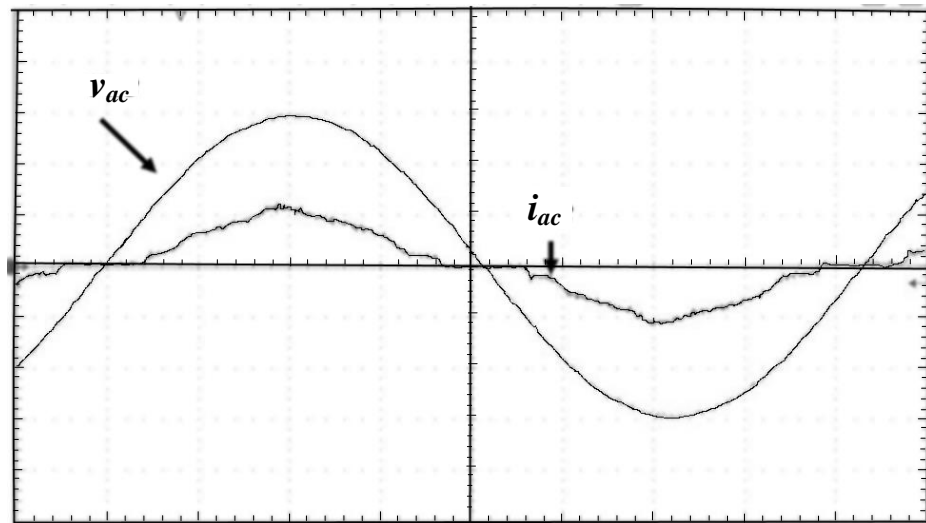


Figure 15. Main line current i_{ac} (200 mA/div) and voltage v_{ac} (60 V/div).

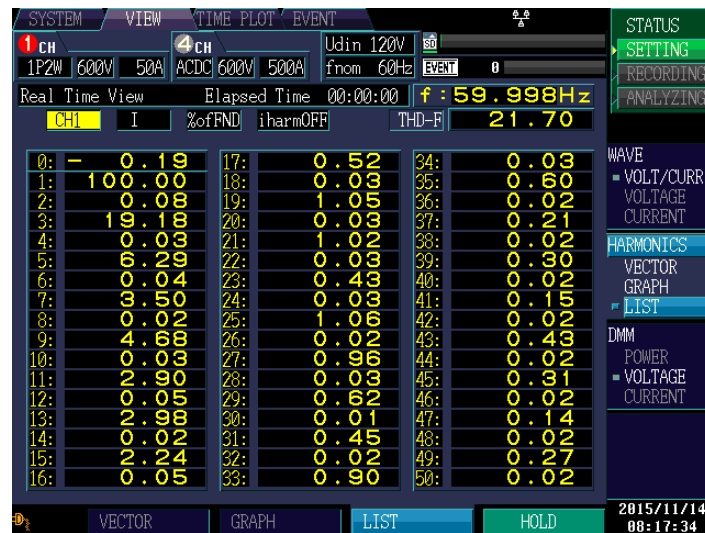


Figure 16. $THDi$ obtained in experimental tests of the power quality meter.



Figure 17. PF obtained in experimental tests of the power quality meter.

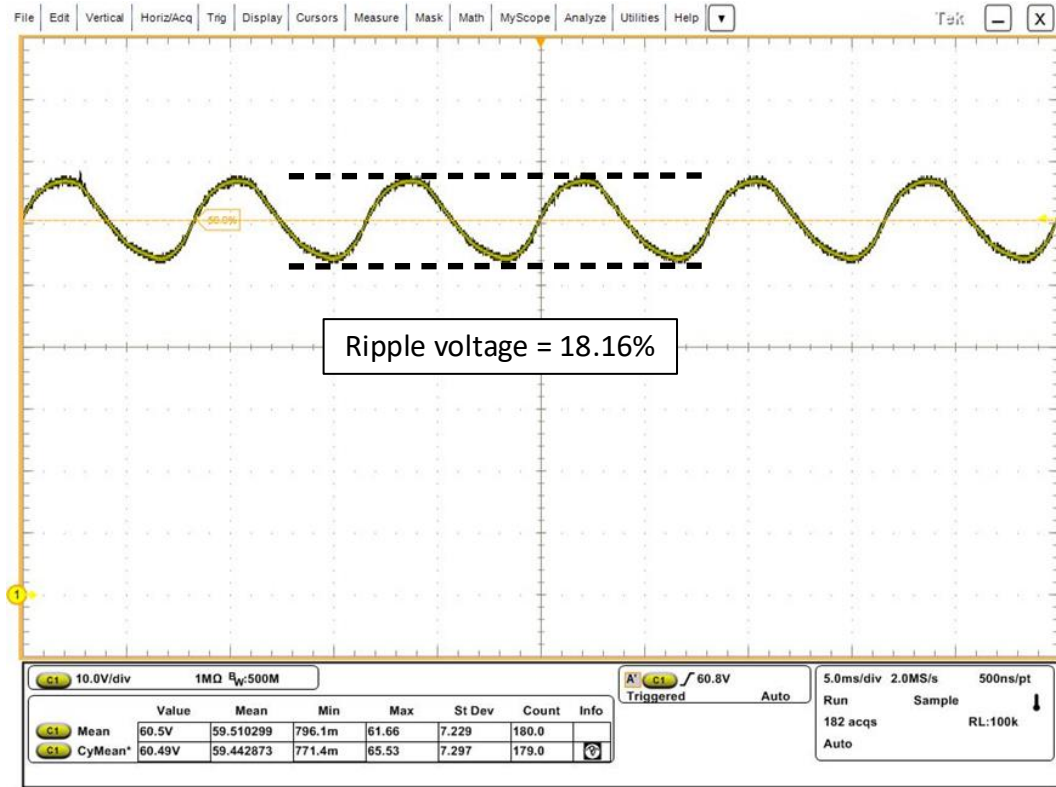


Figure 18. Instantaneous voltage in experimental tests of the LED lamp. 10 V/div, average voltage in the LED 60.5 V.

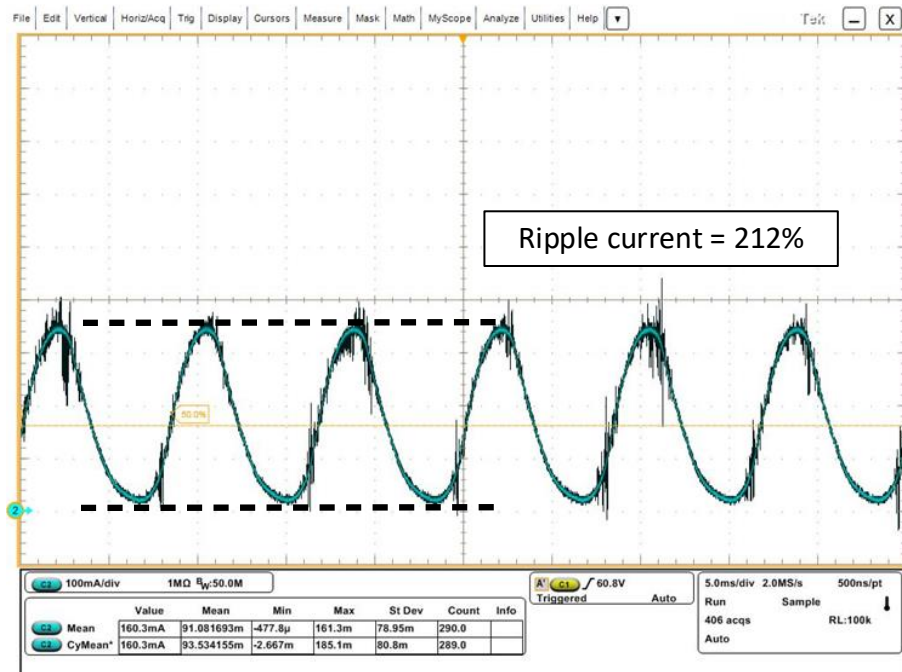


Figure 19. Instantaneous current in experimental tests of the LED lamp. 100 mA/div, average current in the LED 160.3 mA.

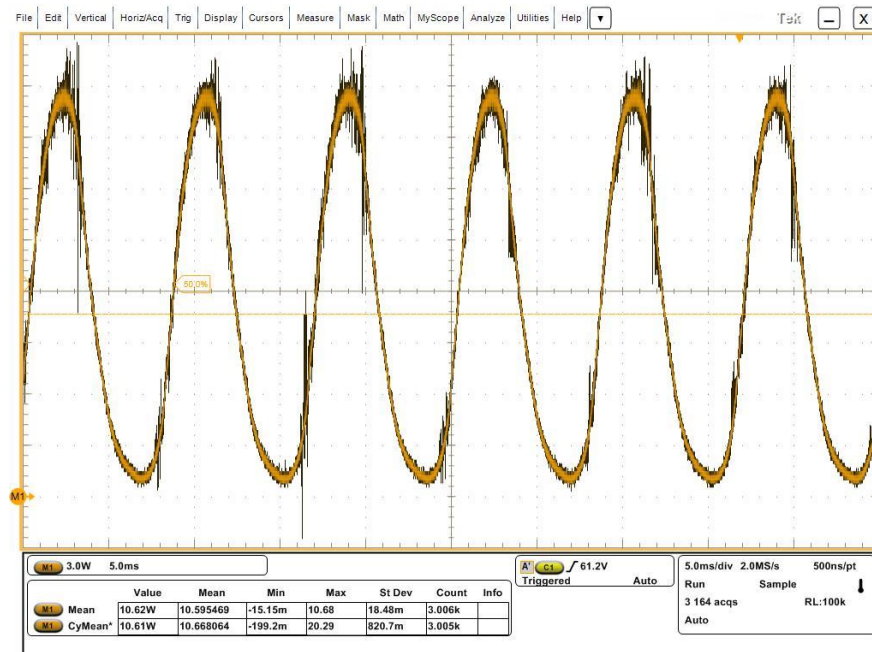


Figure 20. Instantaneous power in experimental tests of the LED lamp. 3 W/div, average power in the LED 10.62 W.

Finally, Tables 5 and 6 summarize what was obtained in the implementation of the topology and the percentages of error obtained, and as expected, there are parameters such as in the case of $THDi$ with a higher percentage of error, this is since losses of the elements used were not considered, in addition to this the construction of the prototype, to mention the manual manufacture of the transformer, which can considerably affect the performance of the entire system.

It should be noted that the flyback only processes 63% of the input power.

Finally, Table 7 shows a small comparison with a couple of similar power topologies. It can be seen that the topology has a good efficiency and power factor compared to the other two topologies, and even less energy stored in the capacitor is reported, which translates into a physically smaller capacitor. However, it has a greater current ripple.

Table 5. Summary of results of the topology.

Parameter	Ideal	PSpice	Prototype
$THDi$	22.58%	19%	21.7%
PF	97.55%	97.9%	96.86%
Average lamp voltage V_{Lam}	60.5 V	60.56 V	60.5 V
Voltage ripple percentage	16%	14.86%	18.16%
Average lamp current I_{Lam}	160 mA	159 mA	163 mA
Current ripple percentage	0	194.8%	212.1%
Average lamp power P_{Lam}	9.68 W	9.62 W	10.61 W
Average rectified power P_i	9.68 W	10.4 W	11.55 W
Processed power Q	60.96%	61.5%	62.94%
Flyback efficiency η_F	95%	90%	88%
Efficiency w/o bridge rectifier η_T	95%	92.5%	91.4%
Efficiency AC line-lamp η_S	95%	90.8%	88.79%

Table 6. Error rates in the topology.

% Error	Ideal-Spice	Ideal-Prototype	Spice-Prototype
$THDi$	−15.85	−3.89	14.21
PF	0.358	−1.014	−1.36
Average lamp voltage V_{Lam}	0.099	0	−0.099
Voltage ripple percentage	−7.25	13.3	22.2
Average lamp current $ILam$	−0.625	0.18175	0.8176
Current ripple percentage	-	-	8.88%
Average lamp power P_{Lam}	−0.6198	9.607	10.29
Average rectified power P_i	7.43	19.3	11.05
Processed power Q	0.885	3.24	2.34
Flyback efficiency η_F	−5	−7.36	−2.2
Efficiency w/o bridge rectifier η_T	−2.63	−3.78	−1.189
Efficiency AC line-lamp η_S	−4.42	−6.53	−2.21

Table 7. Comparison with other reported topologies.

Topology	Potencia de Lámpara	THDi	PF	Efficiency	Current Ripple	Capacitor	Output Voltage	Energy in the Capacitor
[15]	20 W	-	80.3%	80%	14.6%	10 μ F	390 V	760 mJ
[13]	9.8 W	17%	97%	87%	14.1%	4.7 μ F	243 V	138 mJ
This paper	10.61 W	21.7%	96.56	88.79%	212.1%	22 μ F	66 V	47.9 mJ

5. Conclusions

Through this document, a new converter has been evaluated which is based on a variant of the flyback converter and is used as a power supply in solid-state lighting systems.

The proposed converter consists of a rearrangement of the components of the conventional flyback, the secondary is placed in parallel with the LED load and this set is in turn placed in series with the primary and the voltage source.

The primary advantage of this converter is the partial processing of energy, which goes beyond the principle of reduced redundant energy processing (R^2P^2) [16], one part of the energy is directly delivered to the load and the other part is processed by the converter. Since in this rearrangement the flyback converter processed less energy, the stress in the components is lower than in a conventional flyback. As well, this operation allows the efficiency of the proposed converter to always will be greater than the conventional flyback converter. The main disadvantages are the converter have not magnetic isolation, it is a reductive topology and the power factor depends on the gain m of the converter.

The mathematical analysis of the topology of the retrofitted flyback converter was performed and it was shown that it complies with the requirements established by the IEC61000-3-2 class C standard and the FIDE directives in an interval of $0 < m < 0.41$, with a $THDi = 21.7\%$ and a $PF = 0.9686$.

In order to validate the mathematical calculations, a 10 W prototype was built. Experimental results show the rearranged flyback processed only 63% of the input power and the other 37% flows directly to the load.

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